[For : CSE Students]

EC14102 Digital Design	**L-T-P: 2-0-2; Cr: 03**

Pre-requisite: Elements of Electronics Engineering

Objectives/Overview:

This course is intended to provide the students with a good knowledge of all varieties of Digital Circuits (both combinational & sequential circuits) & timing circuits, IC Chips, their design & applications along with Analog to Digital & Digital to Analog conversion of Signals. The lab component indented to make students familiar with all varieties of Digital Circuits (both combinational & sequential circuits) & timing circuits, their design & applications along with Analog to Digital & Digital to Analog conversion.

The students are also exposed to different types of RAMs & ROMs with their in depth knowledge.

Theory Part:

UNIT I: Minimization Technique and Logic Gates **Lectures: 5**

Number Systems, Boolean postulates and laws, De- Morgan's Theorem, Principle of Duality Boolean expression, Minimization of Boolean expressions, Minterm, Maxterm, SOP, POS, Karnaugh map Minimization, Don't care conditions, Quine Mc Cluskey method of min-imization. Binary Codes: Gray Code, BCD Code. Logic Gates: AND, OR, NOT, NAND, NOR, Exclusive OR and Exclusive NOR. Implementations of Logic Functions using gates, NAND–NOR implementations, Multi level gate implementations.

UNIT II: Analysis and Synthesis of Combinatorial Logic Circuits **Lectures: 6**

Adders and Subtractors, Carry look-ahead adders; Multiplexers; De-multiplexers; Encoders; Priority Encoder; Decoders; Code Converters; Magnitude Comparators; Parity generators and Checkers

UNIT III: Sequential Circuits **Lectures: 9**

Sequential Circuit Blocks-Latches, Flip Flops- Race around condition, Master-Slave and edge triggered SR, JK, D & T Flip Flop; Shift Registers; Counters- Synchronous and synchronous, design of ripple counter. Johnson counter, ring counter, sequence generator, Finite state machine (Mealy and Moore Type)

UNIT IV: **Lectures: 10**

Computer Arithmetic & ALU: Structural and functional views of computer system; ALU and data path. Computer arithmetic; ALU data path design for integer addition, subtraction, multiplication and division; Fixed-point and floating-point representations; FPU data path design for floating-point addition, subtraction, multiplication and division; Guard, round and sticky bits in FPU.

UNIT V: **Lectures: 12**

Memory System: Memory system characteristics and design objectives; Memory hierarchy in CISC and RISC systems; Cache memory principle and organization; Cache memory mapping; Cache replacement algorithms; Cache writing policies; Unified and split caches; Random access memory; External memory: disk-based storage and RAIDs, optical storage, SSD storage; Virtual memory, paging and segmentation.
Input/Output Organization: I/O structures and functions; I/O techniques: programmed I/O, interrupt-driven I/O, DMA; Interrupt and interrupt controller; Bus arbitration.

Lab Part: List of Experiments:

1. Universal Gates (i) Identification and verification of NAND gate (IC #7400) and NOR gate (IC #7402). (ii) Construction and Verification of all other gate (AND, OR, NOT, XOR) USING a) Only NAND gate b) Only NOR gate Introduction to SQL: Basic DML, DDL, DTL commands.

2. Code Convertor & Parity Generator and checker. (i) Identification & verification of NOT (7404), AND (7408) OR (7432) & XOR (7486) gates. (ii) Design, construction and verification of 3-bit Binary to Gray convertor and 3-bit Grey to Binary convertor circuit. (iii) Design, construction and verification of 3-bit odd/even Parity Generator and 4-bit odd/even parity checker circuit. Table handling: Alter, Drop Table, Insert Records.

3. Adder, Subtractor & Magnitude comparator circuits. (i) Design, construction and verification of Half Adder and Half Subtractor circuit. (ii) Design, construction and verification of Full Adder and Full Subtractor circuit. (iii) Design, construction and verification of 1-bit and 4-bit Magnitude comparator. (iv) BCD Adder/Subtractor.

4. Decoder, MUX & DMUX (i) Construction and verification of BCD to 7-segment decoder using IC # 7447 (ii) Verification of 4:1 MUX, 8:1 MUX & 16:1 MUX. (iii) Verification of 1:4 DMUX, 1:8 DMUX (iv) Cascading of MUIX and Cascading of Decoders. Join Concept: Simple, Equi, Self, Outer.

5. Latches and Flip Flops (i)Construction and Verification of a Latch circuit using NAND/NOR gates. (ii) Construction and Verification of S-R Flip Flop using above Latch circuits. (iii) Verification of J-K Flip Flop using IC # 7476 (Dual J-KFF) (iv) Construction and Verification of D-Flip Flop and T-Flip Flop using J-K FF (IC #7476). (v) Construction and Verification of Master Slave J-K Flip Flop. Synonym Introduction: Creating object type, Aliasing.

6. Mini project allocation

7. Shift Registers (i) Verification of D-FF using IC # 7474 (Dual D- FF). (ii) Construction and verification of a 2-bit Shift Right Register using IC # 7474 (iii) Construction and verification of a 2-bit Shift Left Register using IC # 7474 (iv) Verification of SISO, SIPO, PISO & PIPO Shift Registers. Introduction to View: create, update, drop.

8. Synchronous & Asynchronous Counters (i) Construction and verification of 2-bit Ripple counter using J-K FF. (ii) Construction and verification of Mod-3 up and Mod-3 down synchronous counter. (iii) Construction and verification of 2-bit Ring counter

using J-K FF. (iv) Construction and verification of 2-bit twisted Ring (Johnson) counter using J-K FF. Introduction to PL/SQL: Advantages, Support, Execution.

9. Design and construction of a 4-bit sequence generator.

Text/Reference Books

1) Digital Systems- Principles & Applications. Tocci, Widmar and Jain, Pearsons
2) Digital Fundamentals. Floyd and Jain, Pearson
3) Digital Circuits (Vol-I & vol-II). D. Roychowdhary, Platinum Publishers.
4) Fundamentals of VHDL Design. Stephen Brown and Zovenkeo Vrasesic, TMH
5) Introduction to Logic Design with CDROM. Alan B. Marcovity, TMH
6) Fundamentals of Digital Logic with Verilog Design. Stephen Brown, TMH
7) Modern Digital Electronics. R. P. Jain, TMH. Problems and solution on Digital circuits (Vol-I & Vol-II). D. Roychowdhary, Platinum Publishers.
8) Andrew S. Tanenbaum, Todd Austin, Structured Computer Organization, Pearson Education, Sixth edition, 2013.

Course Outcomes:

At the end of the course, a student would be able to:

Sl. No.	Outcome	Mapping to POs
1.	Design & implement digital circuits using logic gates IC chips	PO4, PO2
2.	Understand, Design & implement combinational circuits such as logic gates, adder, subtractor, parity generator and checker, Decoder, Multiplexer and De-multiplexer.	PO1, PO2, PO5
3.	Design & implement registers & counters using different flip-flop IC chips.	PO2 , PO3
4.	Analyze and design various analog to digital & digital to analog converters	PO3, PO5
5.	Design digital circuits using MultiSIM	PO1, PO3
6.	Familiarization with basic organizational units of computer	PO4, PO3