Field Effect Transistor – (FET) →

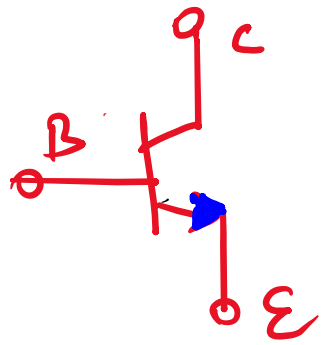
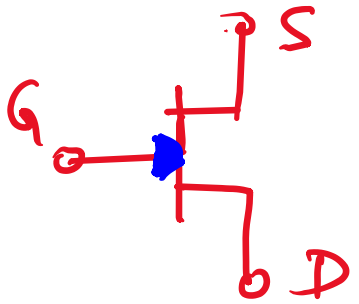
① Junction FET (JFET)

② Metal oxide Semiconductor FET (MOSFET)

We create the channel → (i) Enhancement type MOSFET

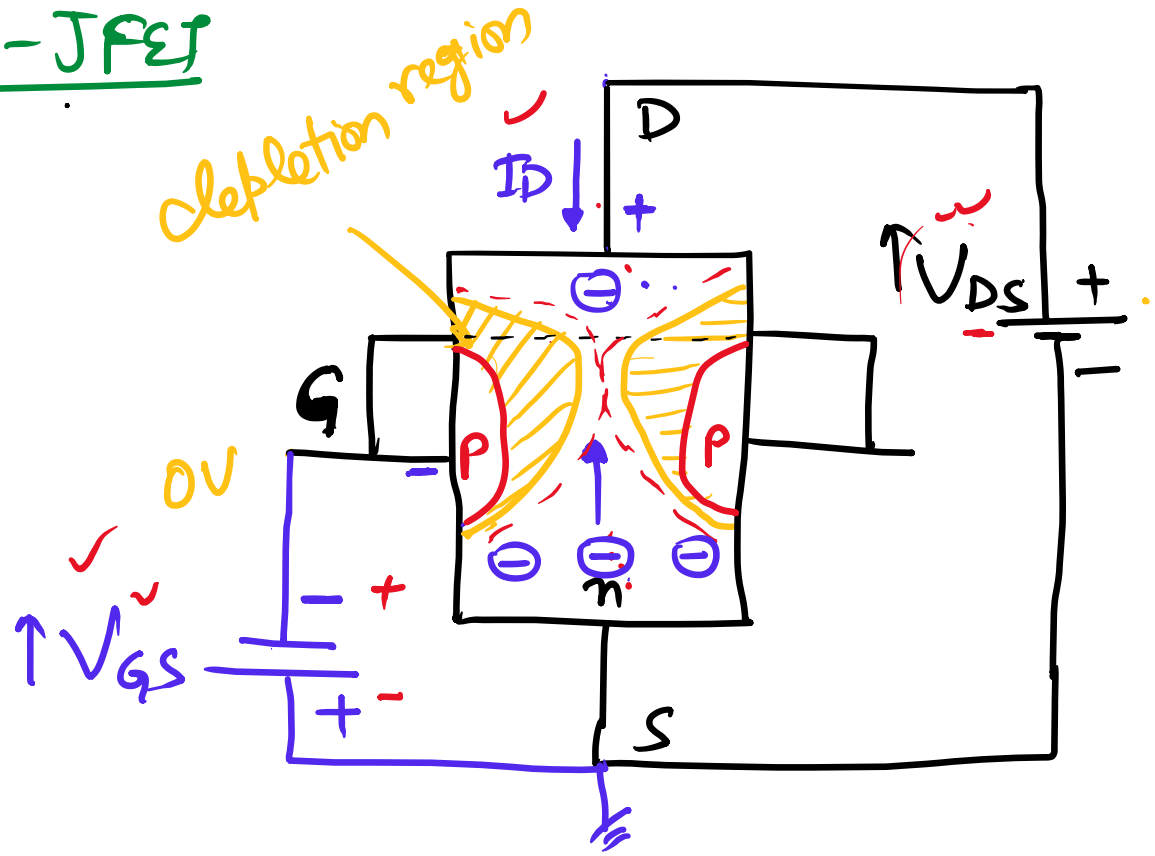
channel is already formed → (ii) Depletion type MOSFET

The difference between BJT & FET →

BJT	FET
①  C - Collector, B - Base, E - Emitter	①  S - Source, D - Drain, G - Gate
② npn & pnp	② n-channel or p-channel.
③ Current controlled device	③ Voltage Controlled device
④ BJT are less temperature Stable.	④ More temperature Stable
⑤ Less input impedance	⑤ provide high input impedance.

Operation & Characteristics of JFET →

n-JFET



① $V_{GS} = 0$, $V_{DS} \uparrow$

→ At the level of V_{DS}, at which the width of depletion region fully covers the channel region..

→ no charge carriers will be flowing from source to drain and $I_D = 0$ ↩ ($V_{DS} = V_p$)

→ This value of V_{DS} at which channel is completely closed is called "pinch off" voltage (V_p)

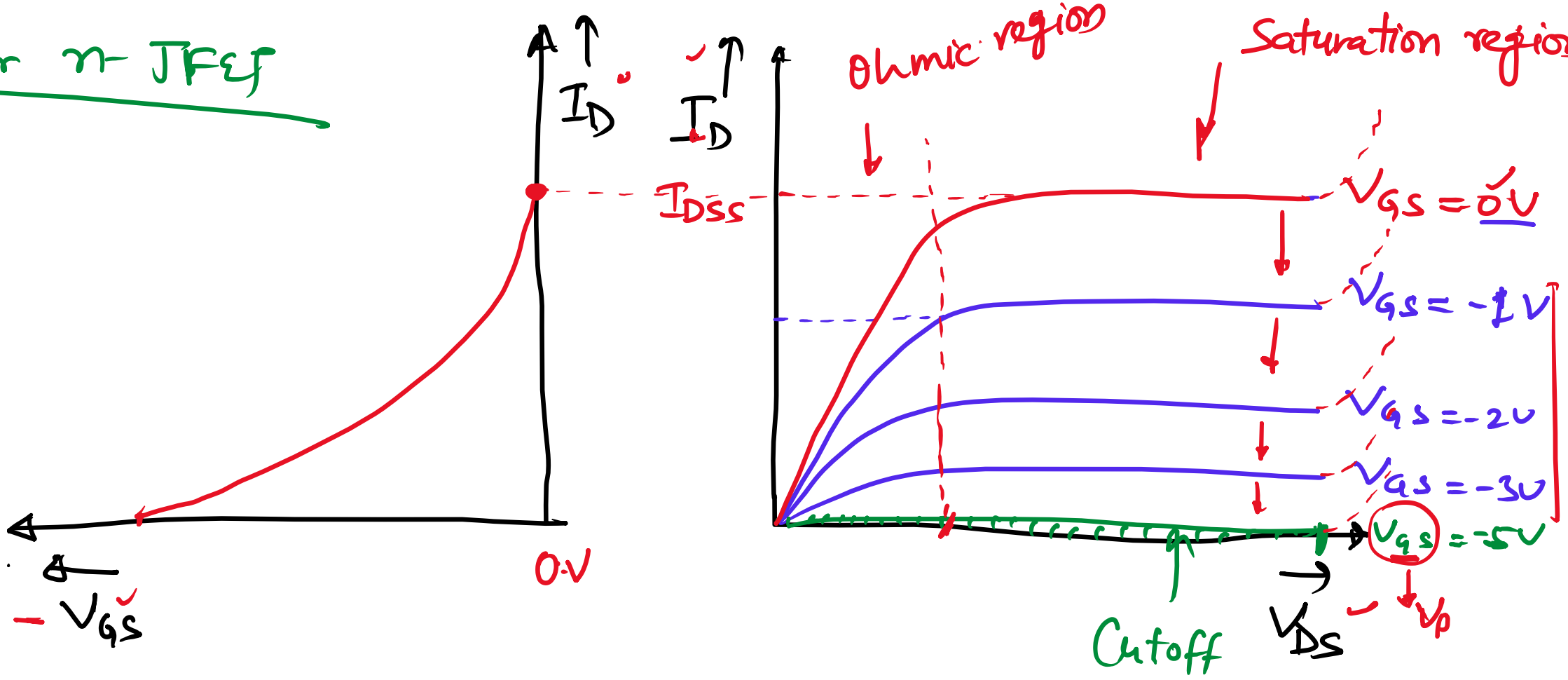
② $V_{GS} \rightarrow$ -ves (negative)

→ The applied negative V_{GS} increases the depletion width due to reverse biased pn junction and V_{DS} attains the level of V_p at smaller values.

→ The current and number of charge carriers is being controlled by V_{GS} & V_{DS} so FET is called voltage controlled device.

Transfer Characteristics of JFET →

For n- JFET



→ Q. Explain the operation for p-type of JFET & also draw the transfer characteristics.

Shockley's Equation-

$$I_D = I_{DSS}\left(1 - \frac{V_{GS}}{V_P}\right)^2$$

V_P ← Pinch-off Voltage.

at $V_{GS} = 0V$ $\Rightarrow$ $I_D = I_{DSS}(1-0)^2 = I_{DSS}$

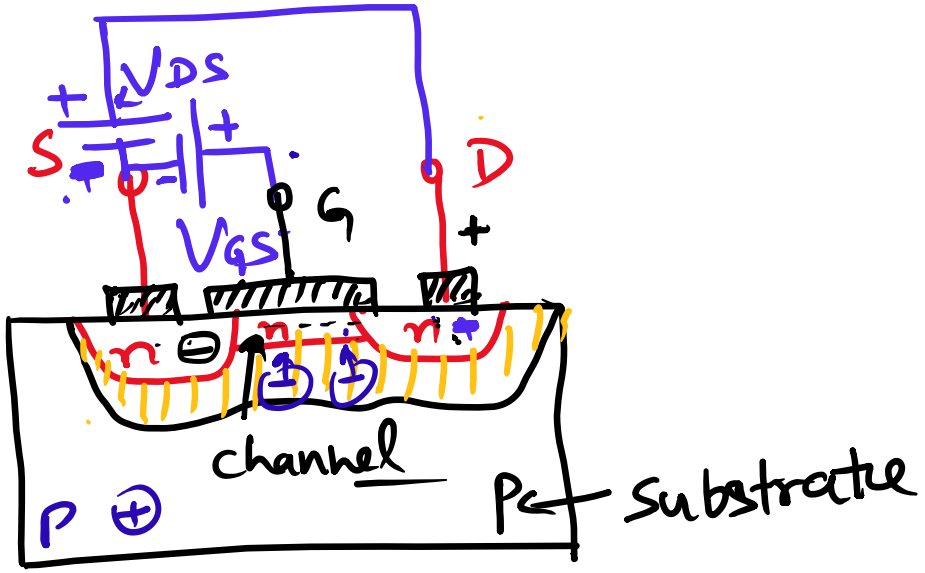
at $V_{GS} = V_P$ $\Rightarrow$ $I_D = I_{DSS}(1-1)^2 = 0$

* In FET's Gate is always reverse biased.

Metal oxide Semiconductor FET (MOSFET)→

① Depletion type MOSFET → P-channel
n-channel.

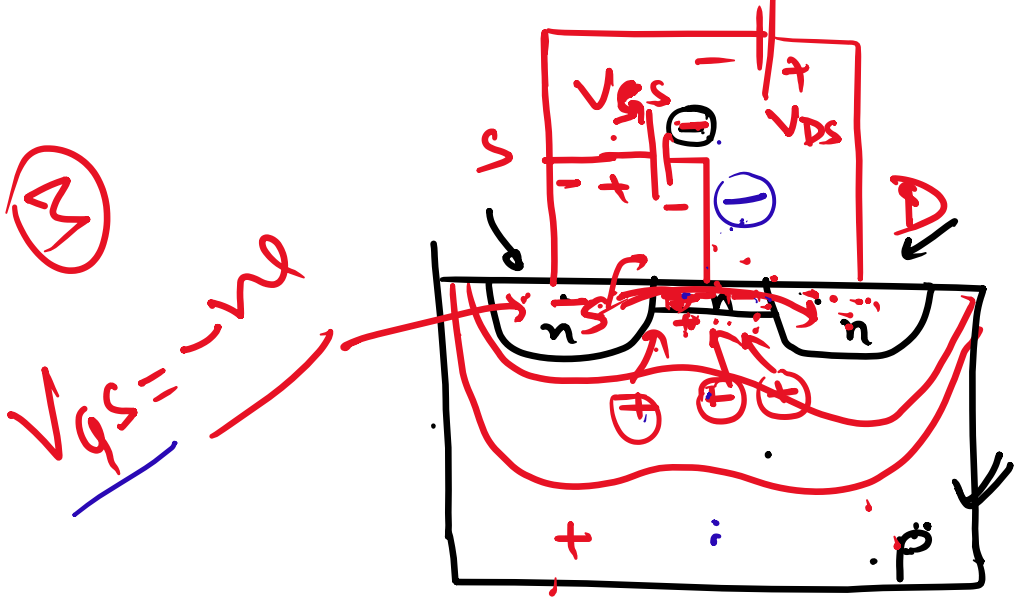
(channel is already formed)



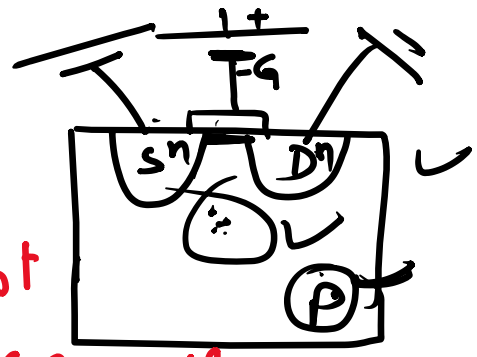
① $V_{GS} = 0V$, V_{DS} ↑

② V_{GS} → +ve ✓

→ for large value of applied V_{GS} for which depletion layer is sufficiently large to close the channel then Pinch-off occurs.

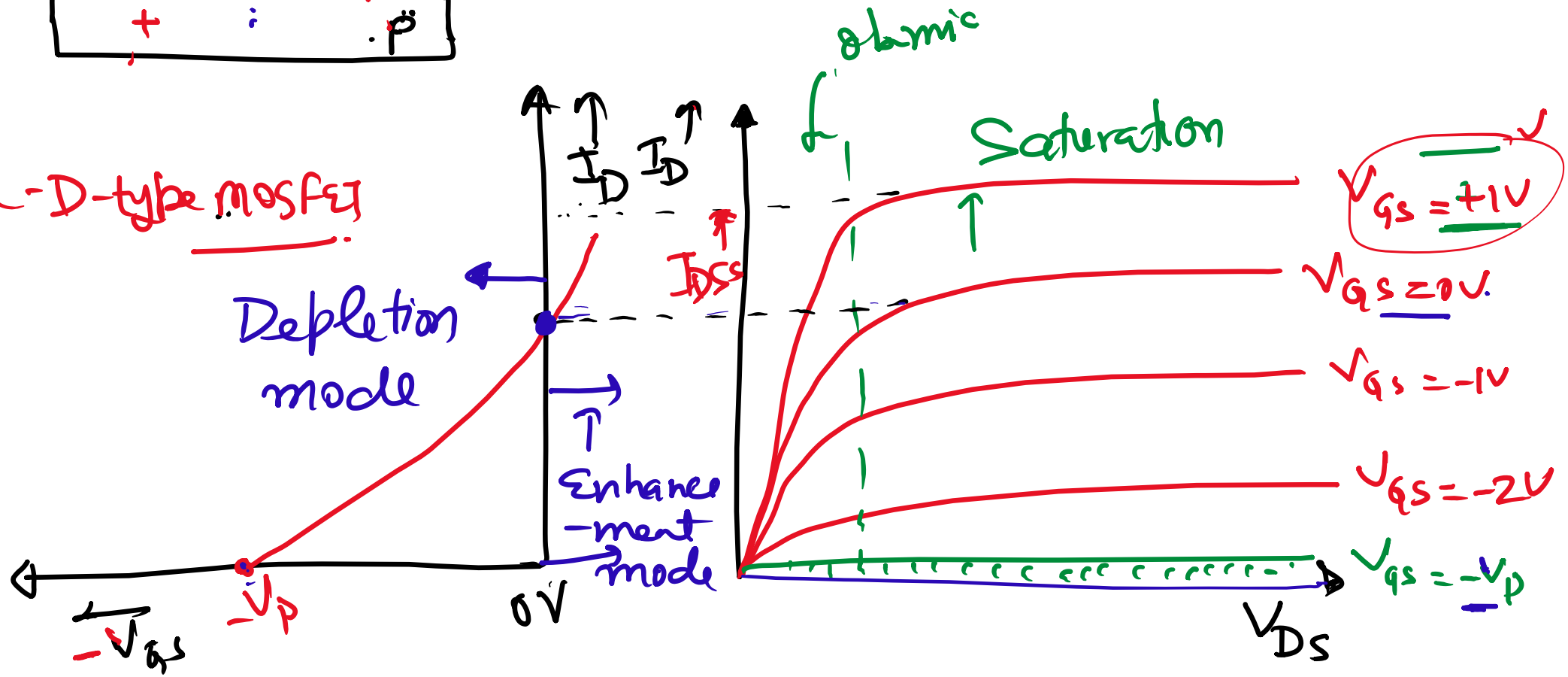


$V_{GS} = 0V$



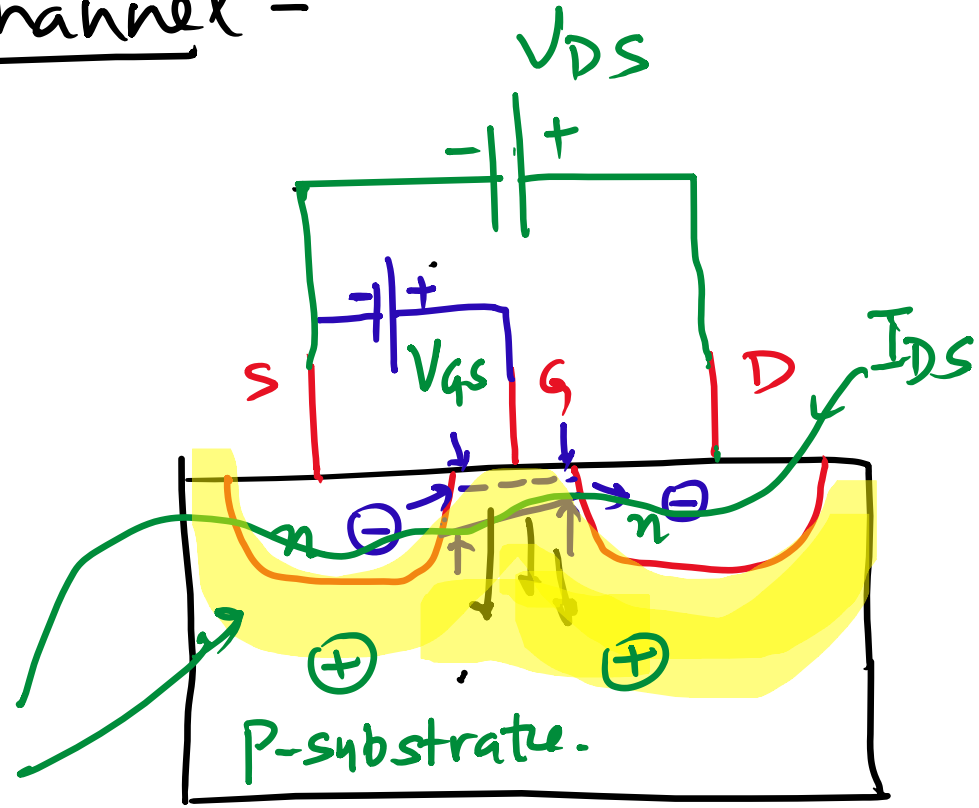
Channel can't not Create charge carrier

Q p-channel-D-type mosfet



② Enhancement type MOSFET → (i) n-channel (ii) P-channel.

① n-channel –



① $V_{GS} = 0V$

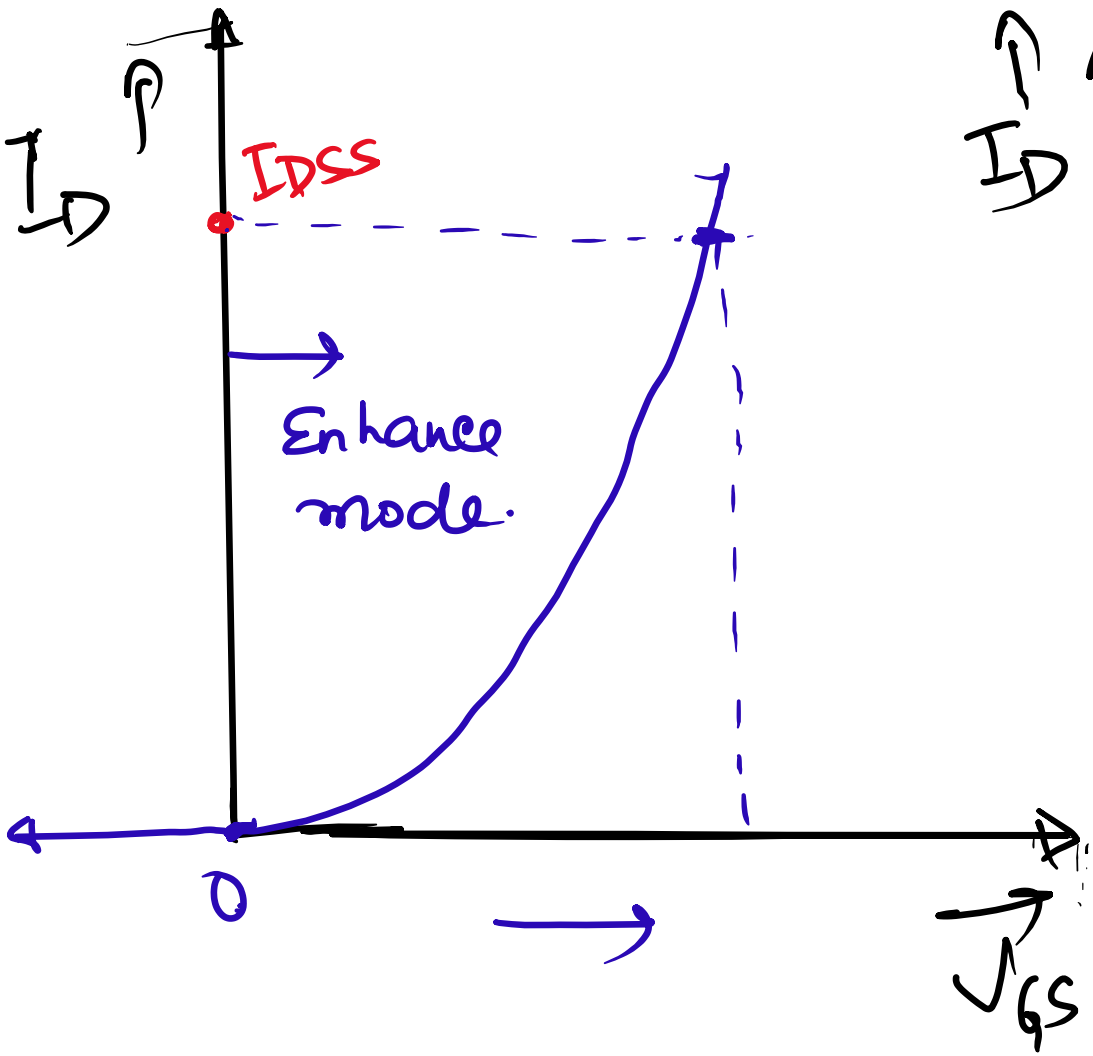
② $V_{GS} \Rightarrow +ve$ V, $V_{DS} \Rightarrow +V_{DD}$

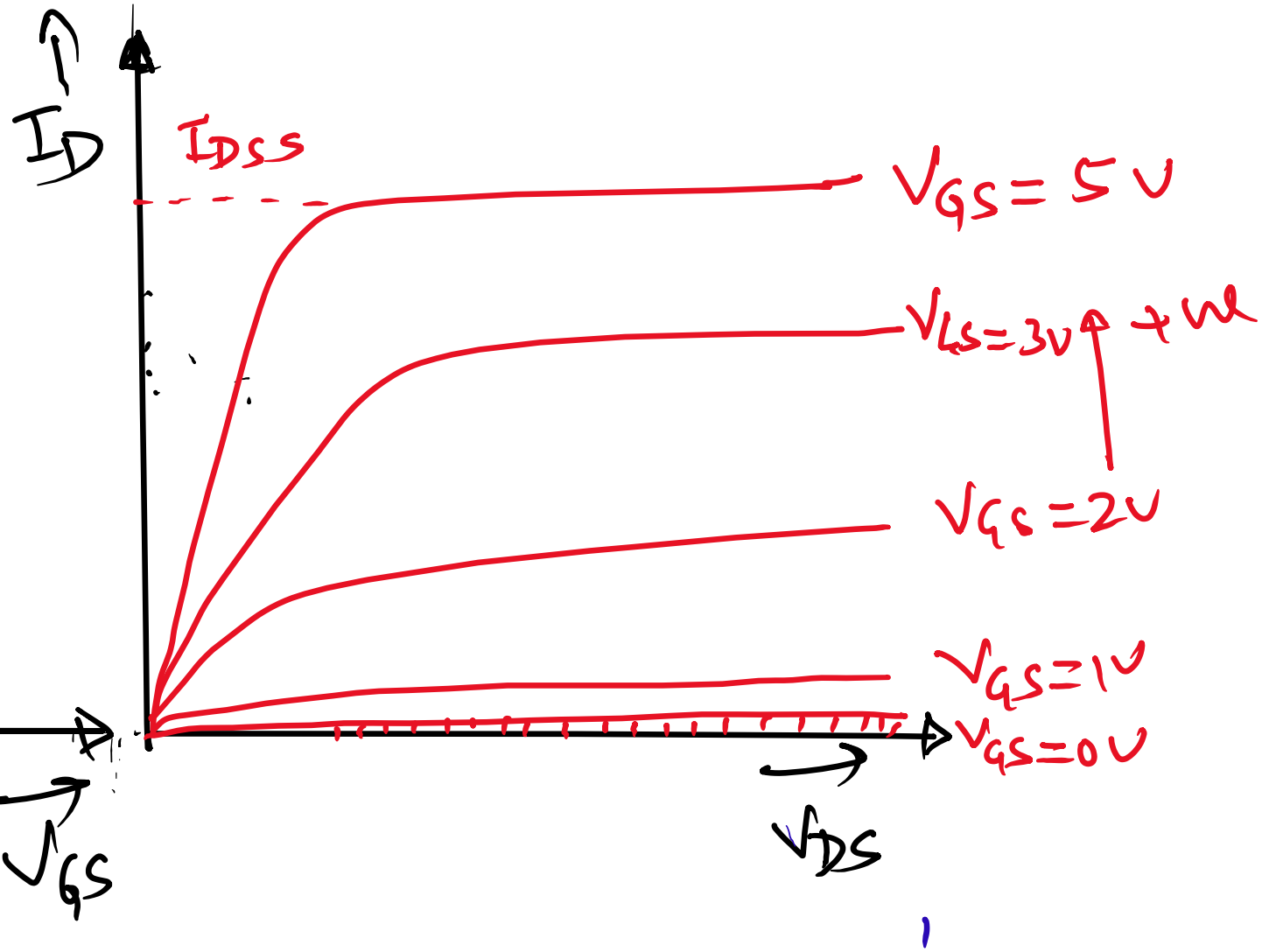
→ Channel is formed due to accumulation of e^-s near the gate terminal.

③ $V_{GS} \Rightarrow -ve$, V_{DS}

e^- of channel region will be repleled. and depletion region will be created.

Transfer characteristics -





JFET →
- Fixed bias
- Self bias
- Potential divider bias
- Common gate
- JFET ⇒ ($R_D = 0$) } - special cases.
- $V_{GSQ} = 0V$

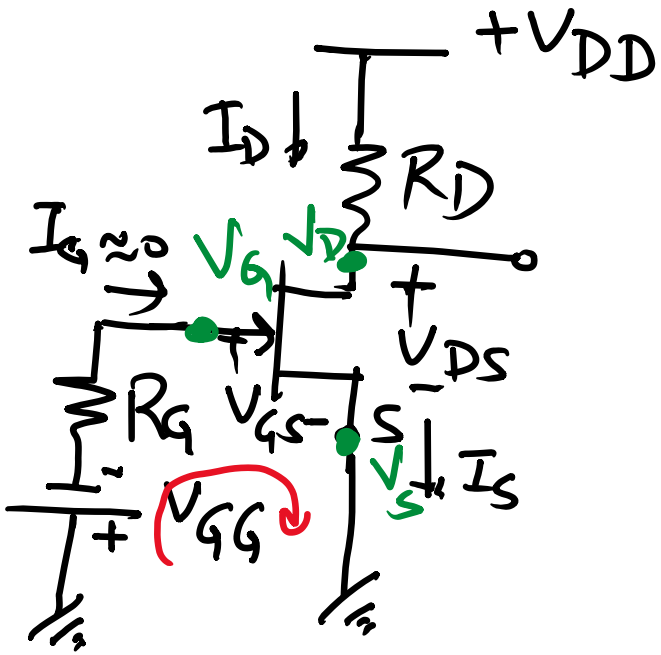
Depletion type MOSFET

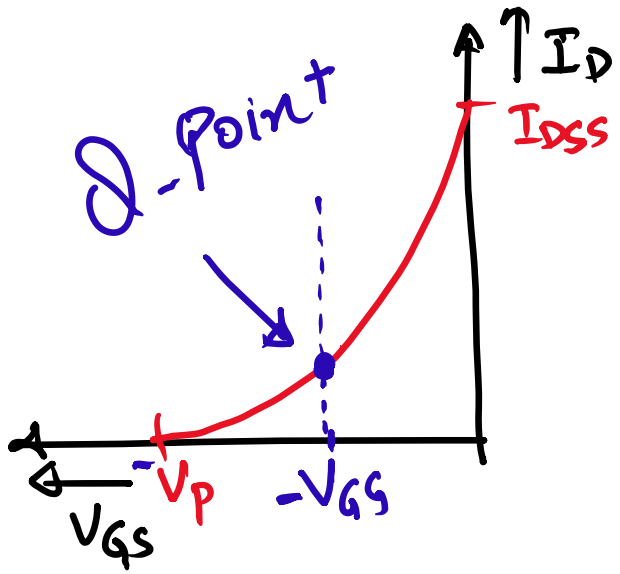
1. Fixed bias
2. Potential divider bias

Enhancement type -

1. Feedback Configuration
2. Potential divider bias

① Fixed bias (JFET) → (Common Source Configuration)





① $I_G \simeq 0 \Rightarrow I_D = I_S$

$+V_{GG} + V_{GS} = 0 \Rightarrow \boxed{V_{GS} = -V_{GG}}$ — ①

$-V_{DD} + I_D R_D + V_{DS} = 0$ — ②

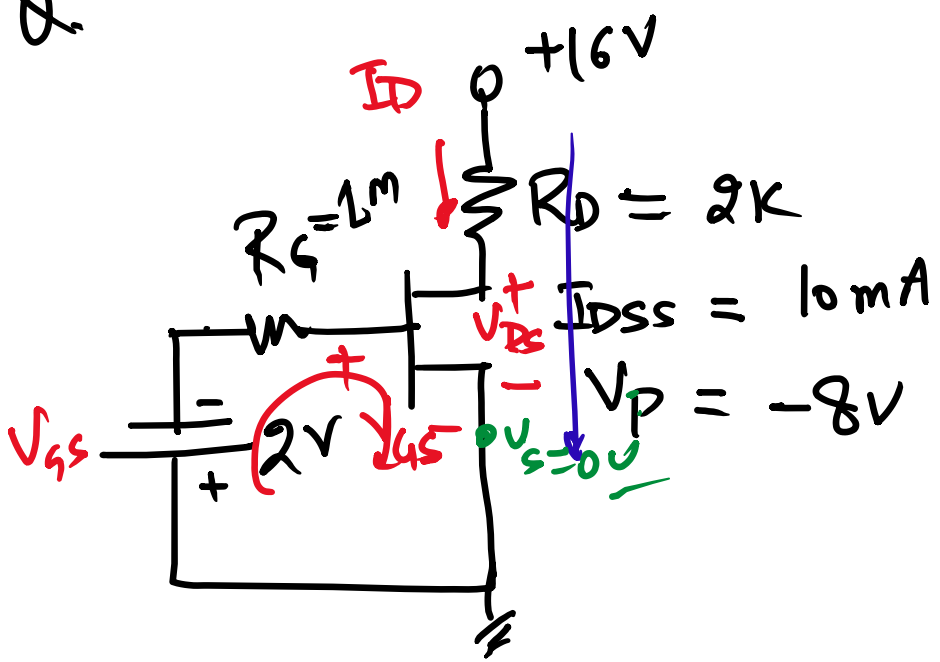
$$\boxed{V_{DS} = V_{DD} - I_R R_D}$$

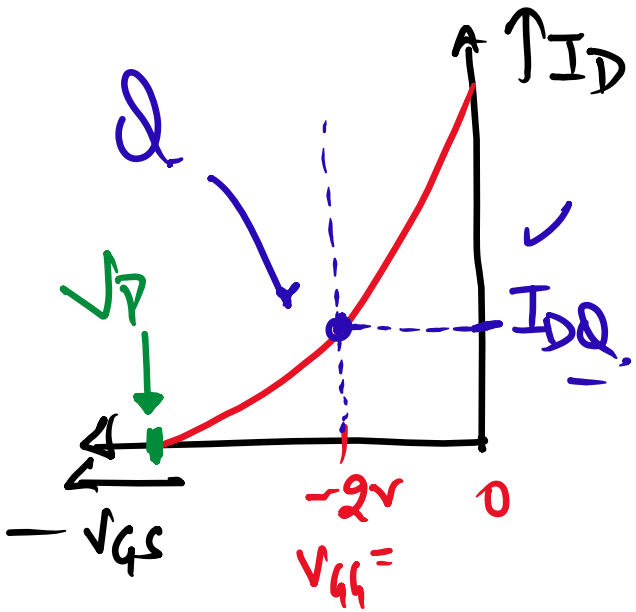
$\Rightarrow V_{DS} = V_D - V_S \Rightarrow V_S = 0$ (F.B.)

$V_{DS} = V_D$

$\Rightarrow V_{GS} = V_G - V_S \Rightarrow \underline{V_{GS} = V_G}$

Q.





Determine -

V_{GSQ}, I_{DQ}, V_{DS}, V_D, V_G, V_S.

Sol: ① $I_G = 0 \Rightarrow I_D \approx I_S$

$+2 + V_{GS} = 0 \Rightarrow \boxed{V_{GS} = -2V}$

$$I_D = I_{DSS}\left(1 - \frac{V_{GS}}{V_P}\right)^2 = 10\times10^{-3}\left(1 - \frac{(-2)}{(-8)}\right)^2$$

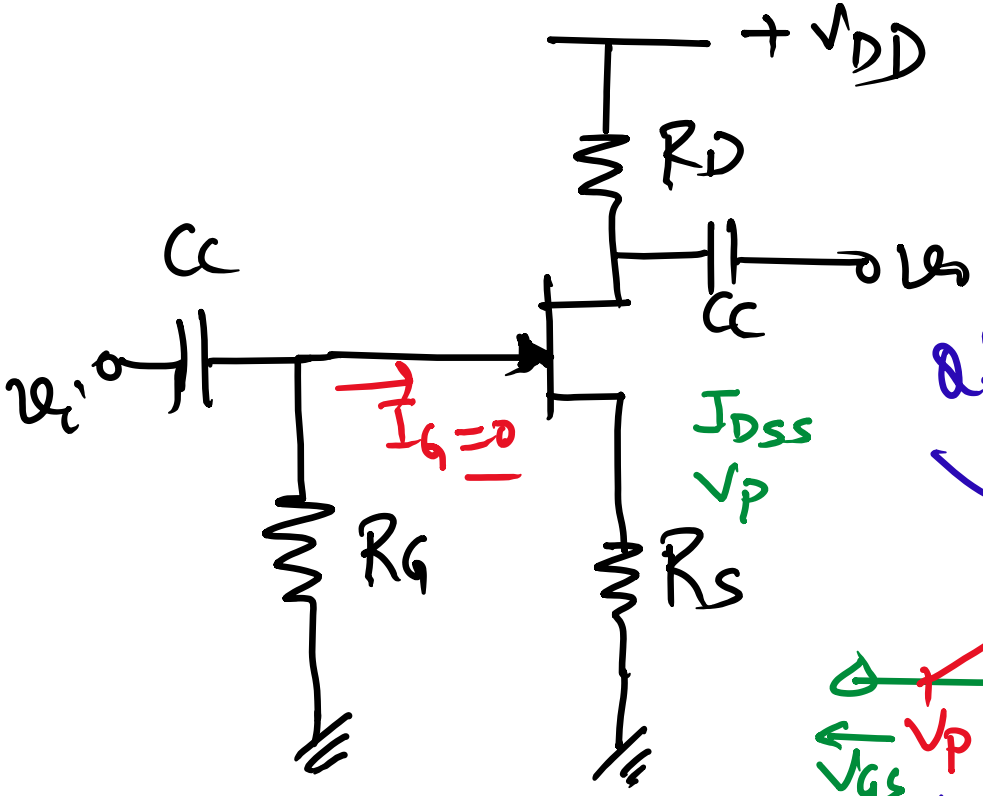
$$-16 + I_D R_D + V_{DS} = 0$$

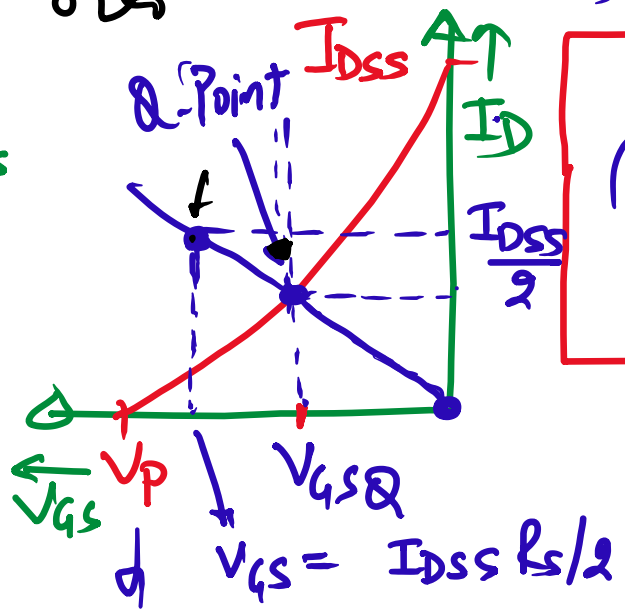
$\Rightarrow V_{DS} = V_D - V_S$, $V_{GS} = V_G - V_S$

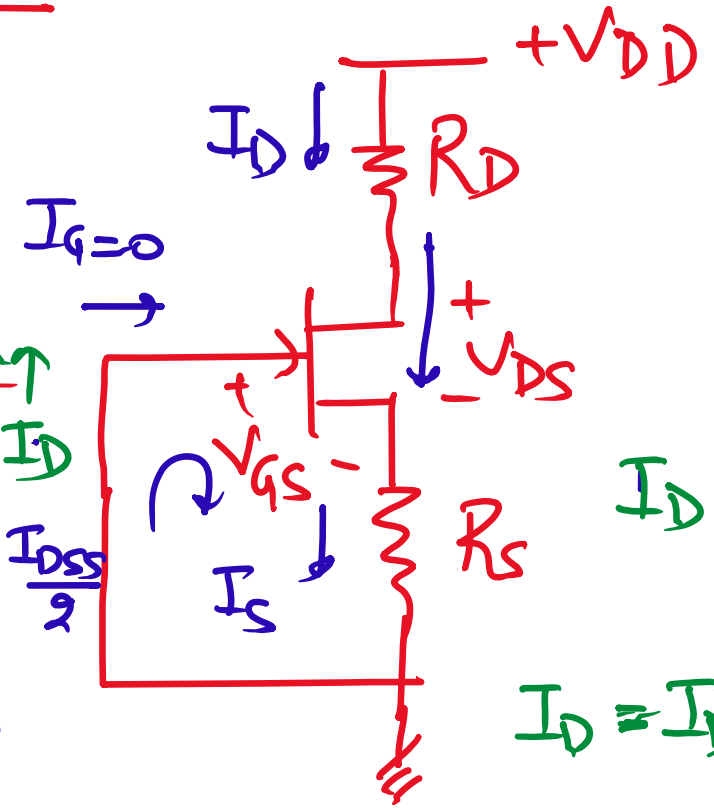
$\rightarrow V_S = 0V$

② Self bias →

$I_G = 0 \Rightarrow I_D = I_S$







$V_{GS} + I_S R_S = 0$

$V_{GS} = -I_D R_S$ ①

$$I_D = I_{DSS}\left(1 - \frac{V_{GS}}{V_P}\right)^2$$

$$I_D = I_{DSS}\left(1 + \frac{I_D R_S}{V_P}\right)^2$$

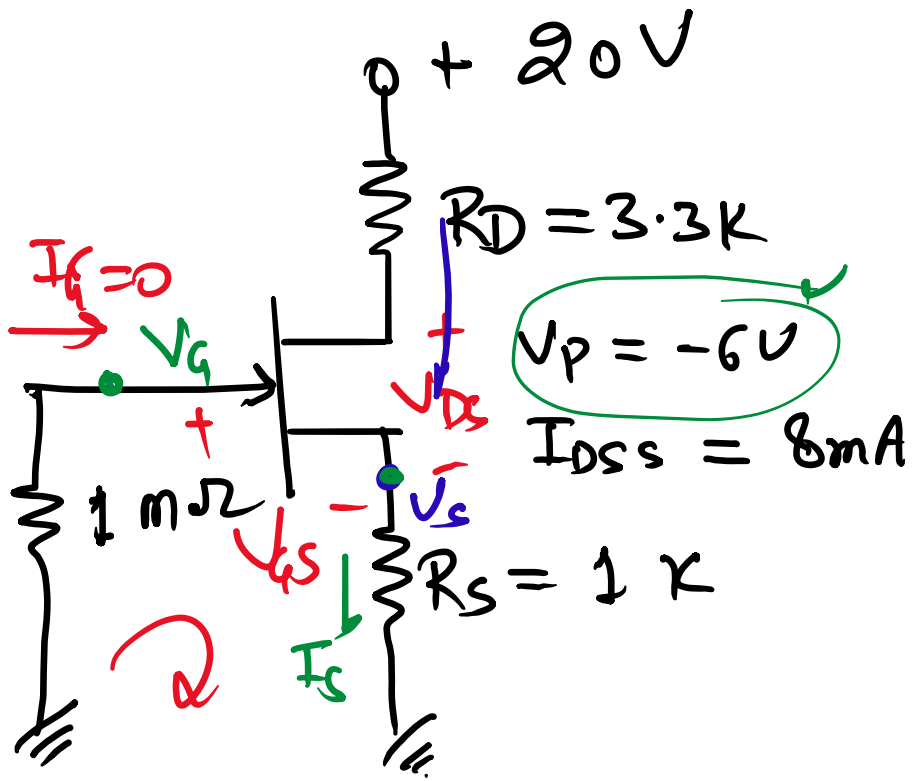
$I_D = \alpha, \beta$

$-V_{DD} + I_D R_D + V_{DS} + I_D R_S = 0$

$$V_{DS} = V_{DD} - I_D(R_D + R_S)$$ ②

$$I_D \simeq \frac{I_{DSS}}{2} \rightarrow V_{GS} = -\frac{I_{DSS} R_S}{2}$$

Q.



$I_D = I_S$ | $I_G = 0$

$V_{GS} = -I_D \cdot R_S$

$I_D = \frac{I_{DSS}}{2} \approx \frac{8}{2} = 4mA$

$V_{GS} = -4 \times 10^3 \times 10^{-3} = -4V$

Determine - V_{GSQ}, I_{DQ}, V_{DS}, V_S, V_G & V_D.

$-20 + I_D \times 3.3 \times 10^3 + V_{DS} + 10^3 \times I_D = 0$

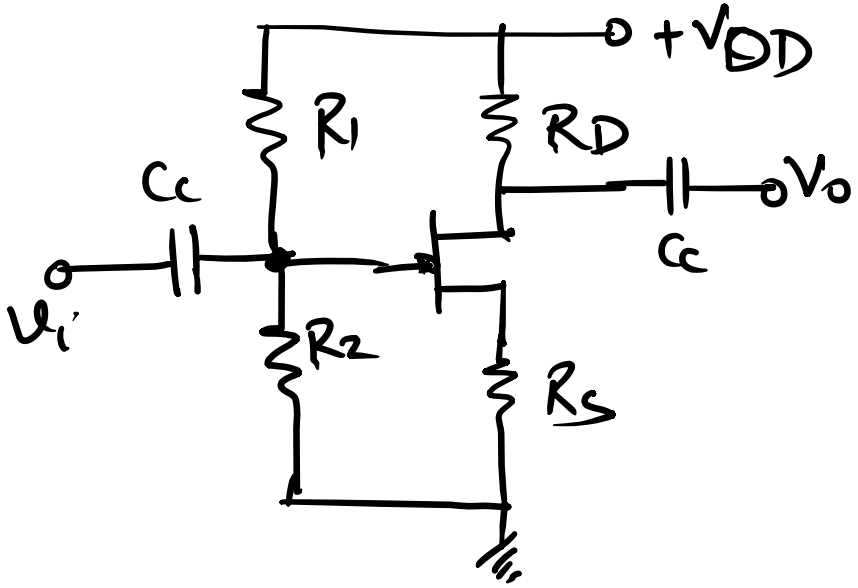
$V_S = I_S R_S = I_D R_S$

$V_G = 0V$

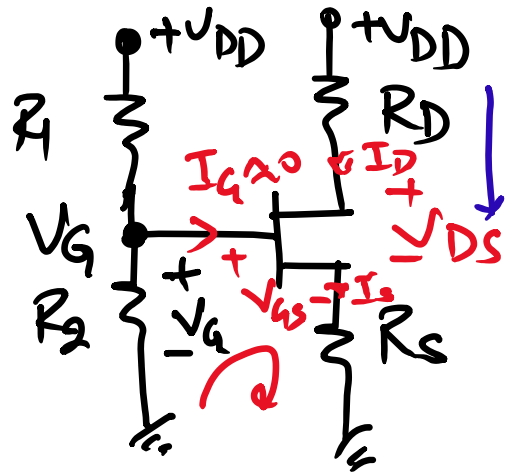
$V_{DS} = V_D - V_S$

③ Potential divider biasing (JFET) →

$I_G \approx 0 \Rightarrow I_D \simeq I_S$



DC Analysis

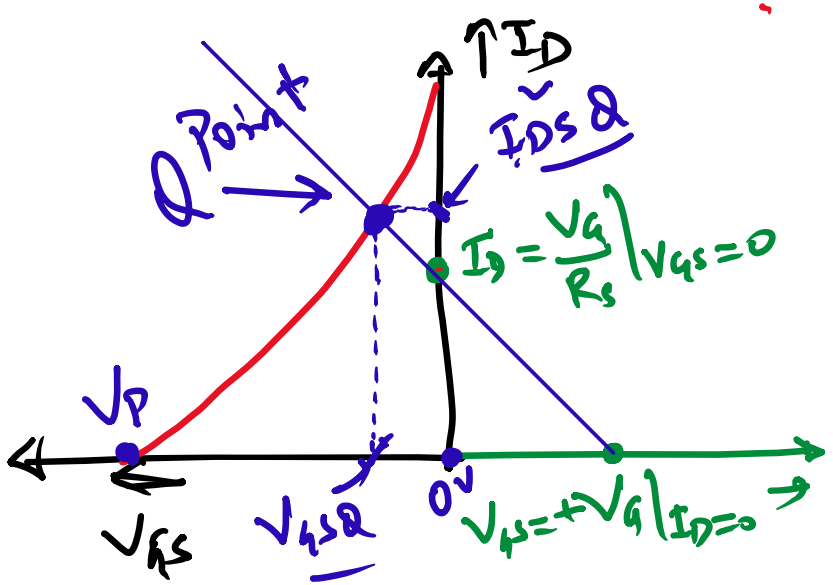


Thomin's theorem

$$V_G = +\frac{V_{DD} R_2}{R_1 + R_2}$$

$$-V_G + V_{GS} + I_D R_S = 0$$

$$\boxed{V_{GS} = V_G - I_D R_S} \quad -①$$



Conditions

$$-\tilde{V}_{DD} + \tilde{I}_D R_D + \tilde{V}_{DS} + \tilde{I}_D R_S = 0$$

$$\Rightarrow \boxed{V_{DS} = V_{DD} - I_D(R_D + R_S)} \quad ②$$

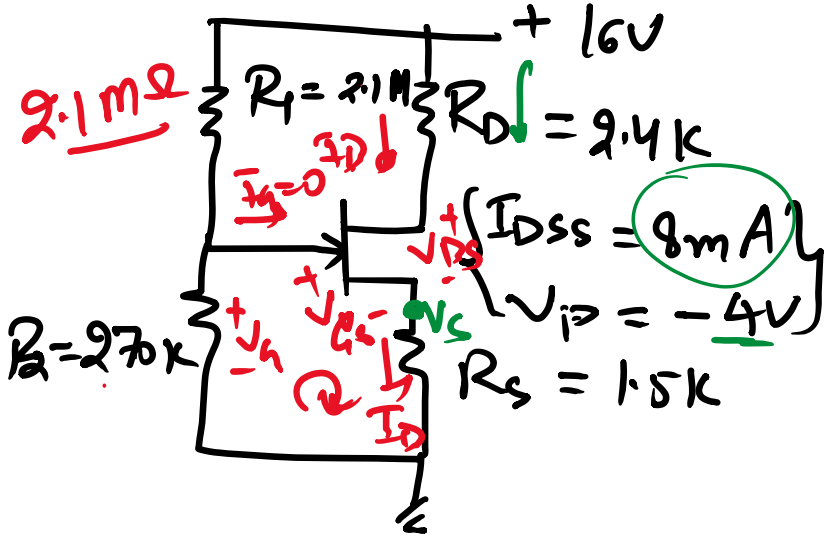
① $I_D = 0$

$V_{GS} = \pm V_G$

② $V_{GS} = 0$

$0 = V_G - I_D R \Rightarrow I_D = \frac{V_G}{R_S}$

Q Determine → I_{DQ}, V_D, V_{GSQ}, V_S, V_{DS}, V_{DG}

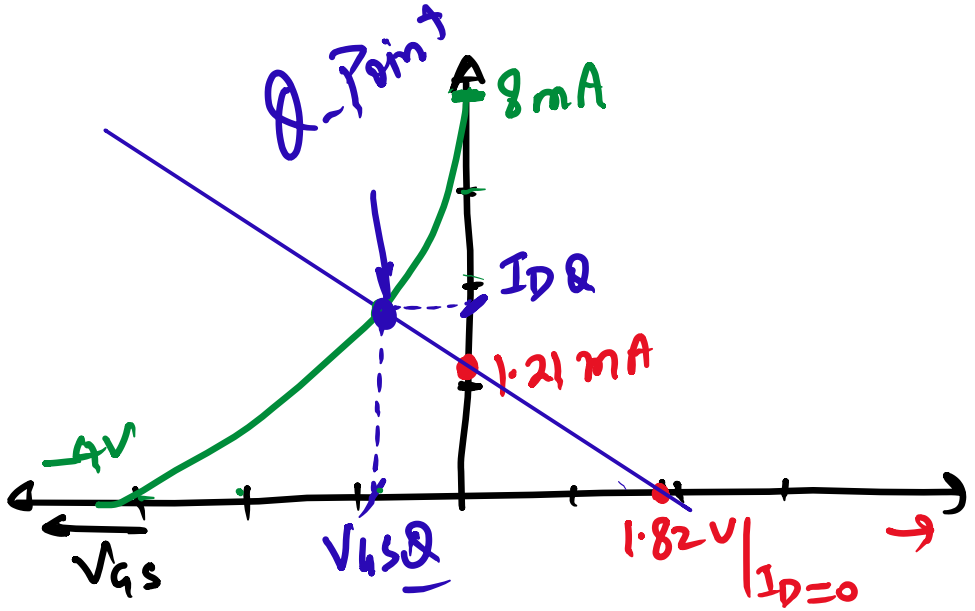


$$V_G = \frac{+V_{DD} R_2}{R_1 + R_2} = 1.82\,V$$

$$-V_G + V_{GS} + I_D R_S = 0 \Rightarrow V_{GS} = V_G - I_D R_S$$

① $I_D = 0 \Rightarrow V_{GS} = V_G$

② $V_{GS} = 0 \Rightarrow I_D = V_G / R_S = 1.82 / 1.5 \times 10^{3} = 1.21\,mA$



$$\Rightarrow I_{DQ} = 2.4\,mA$$
$$\leftarrow V_{GSQ} = -1.8\,V$$

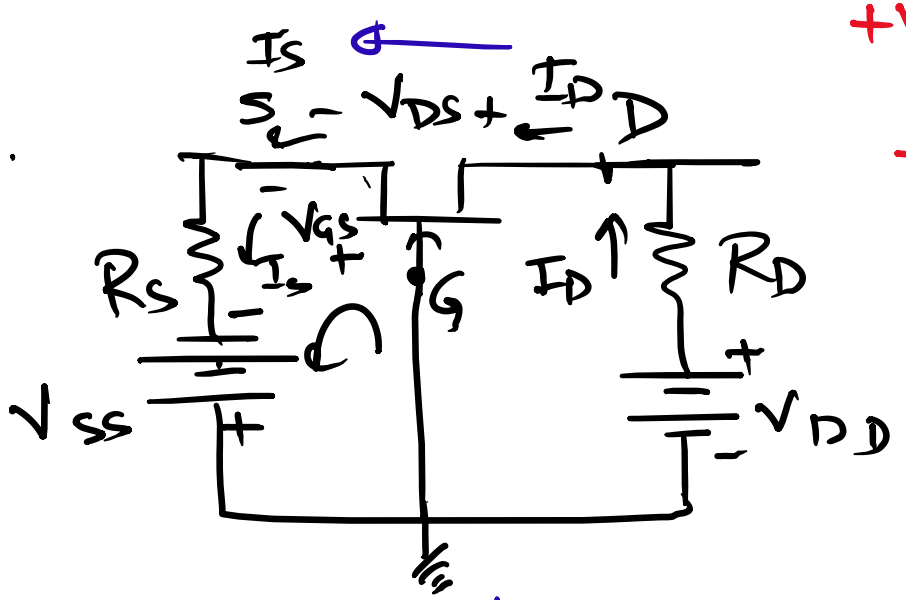
$$-V_{DD} + I_D R_D + V_{DS} + I_D R_S = 0 \Rightarrow V_{DS} = ?$$

$$V_{DS} = V_D - V_S$$

$$V_{DG} = V_D - V_G$$

④ Common Gate Configuration -

$I_G = 0 \Rightarrow I_D = I_S$



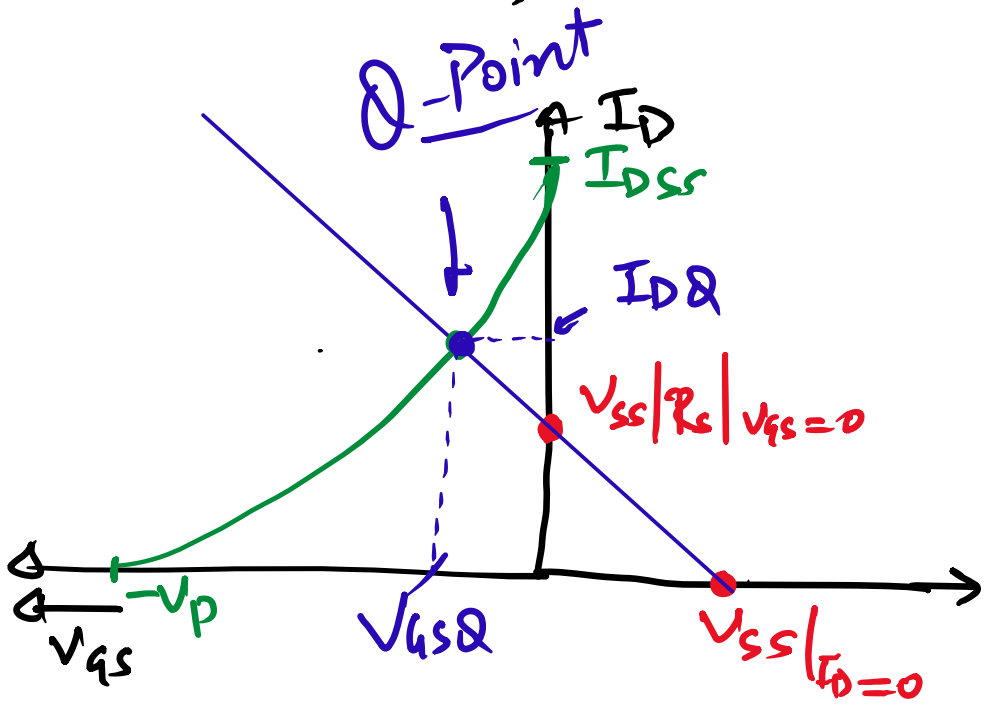
$$+V_{GS} + I_S R_S - V_{SS} = 0$$

$$\Rightarrow \boxed{V_{GS} = V_{SS} - I_D R_S} \quad -(1)$$

① $I_D = 0 \Rightarrow V_{GS} = +V_{SS}$

② $V_{GS} = 0 \Rightarrow I_D = +V_{SS}/R_S$

$\Rightarrow I_{DSQ}$, V_{GSQ} ← using graphical method.

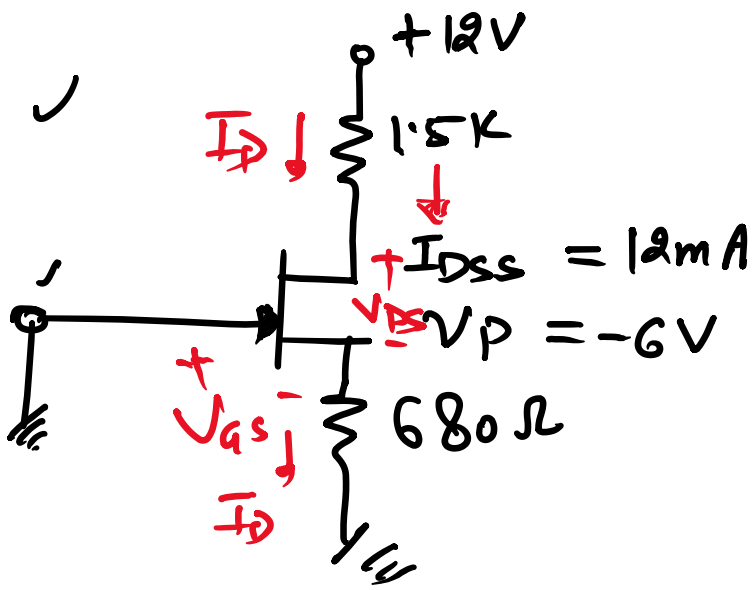


$$-V_{DD} + I_D R_D + V_{DS} + I_D R_S - V_{SS} = 0$$

$\Rightarrow V_{DS} = ?$

Q Determine → V_{GSQ}, I_{DQ}, V_D, V_G, V_S & V_{DS}

$I_G = 0 \Rightarrow I_D = I_S$



$\Rightarrow V_{GS} + I_D R_S = 0 \Rightarrow$ $V_{GS} = -I_D R_S$ — (1)

① $I_D = 0 \Rightarrow$ $V_{GS} = 0V$

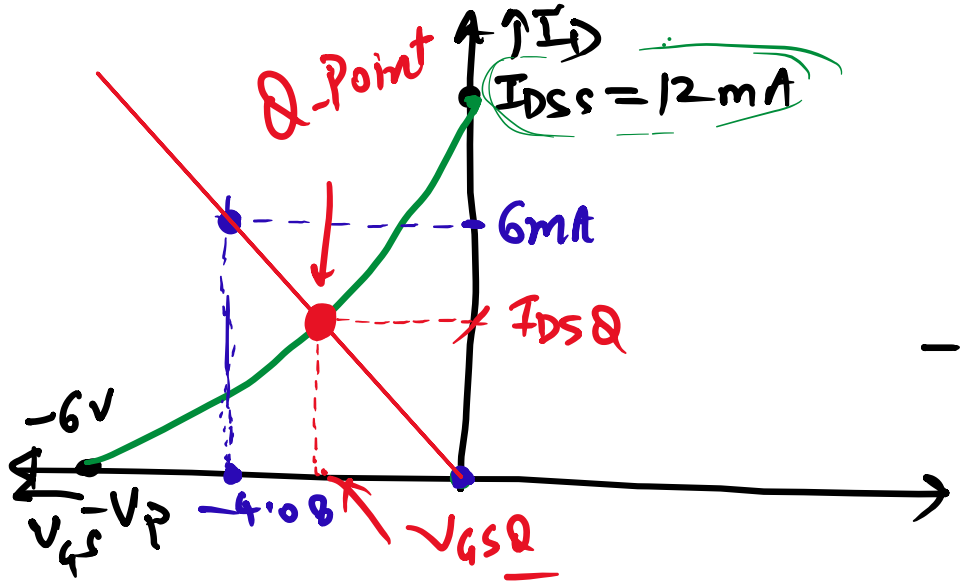
② $V_{GS} = 0 \Rightarrow$ $I_D = 0$

[Assume any value of I_D { $I_D \simeq I_{DSS}$ or $\frac{2}{4} I_{DSS}$ }

$I_D = 6mA$

$V_{GS} = -6 \times 680\,\Omega \times 10^{-3} = -4.08V$

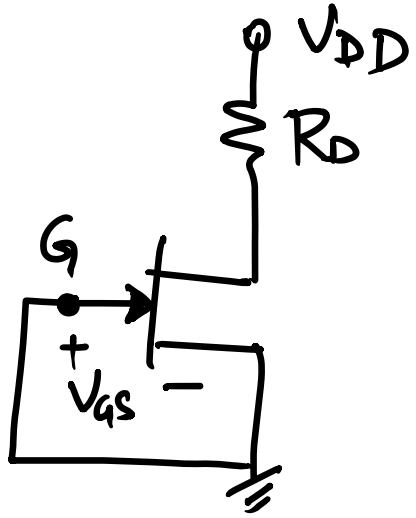
$V_{GS} \simeq -2.6V$ & $I_{DQ} = 5.8mA$



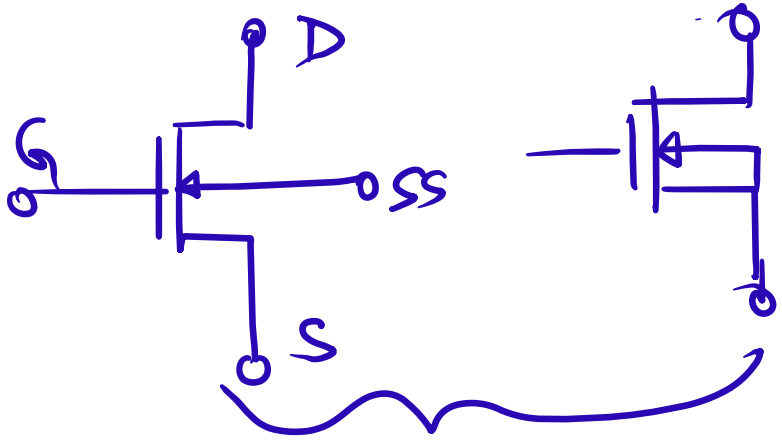
$-12 + 1.5 \times 10^3 \times I_D + V_{DS} + 680 \times I_D = 0 \Rightarrow V_{DS} = ?$

$V_S = I_D R_S$ $\Rightarrow V_{DS} = V_D - V_S$, & $V_G = 0V$

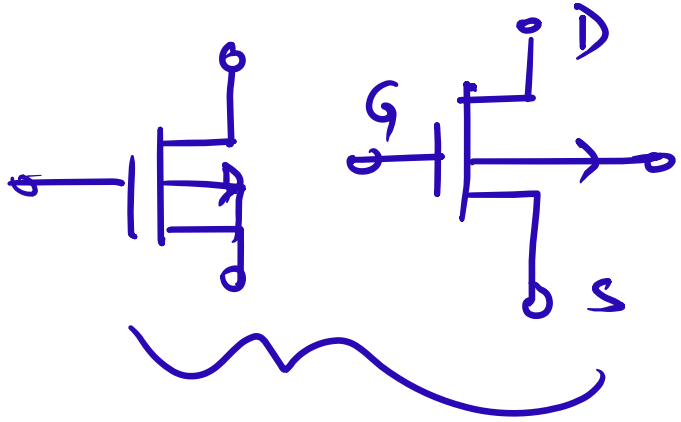
⑤ Special Cases - $V_{GSQ} = 0\ V$



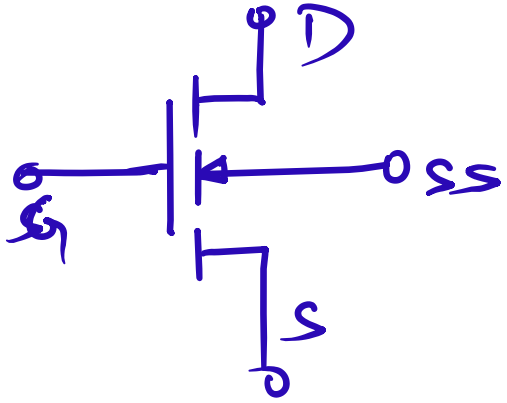
{ Study Special Cases.
4 Depletion & Enhancement type MOSFET biasing. }

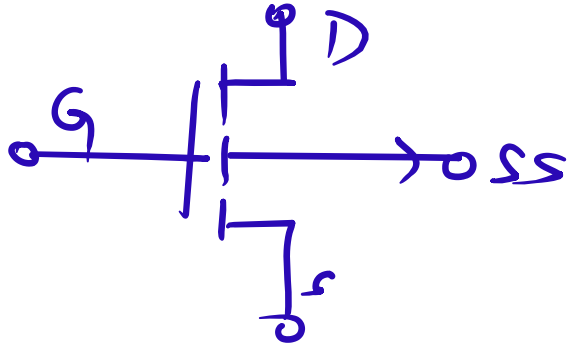


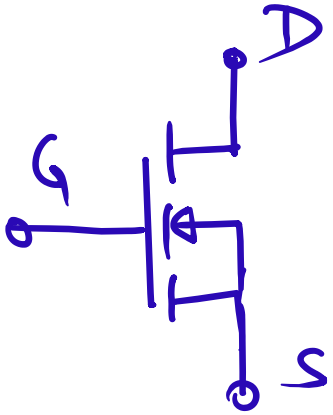
n-channel depletion type MOSFET

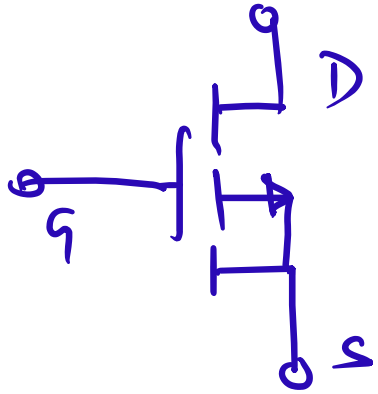


p- Channel









n-chanel Enhancement type MOSFET

P-channel Enhancement type mosfet.