NATIONAL INSTITUTE OF TECHNOLOGY PATNA
END SEM EXAM 2024 B. Tech Sem-I, Elements of Electronics (EC16102), 3 hour, 60 marks

Attempt all the questions.

Q1 attempt all (20 marks)

i. The reverse saturation current is of $20\mu A$ in a PN junction diode at room temperature. What will be its values after 20° rise in the temperature? (2 marks, BL: L3, PO: 2)

ii. Draw the circuit of positive clipper with the offset value of 2V and explain its operation. (2 marks, BL: L2, PO: 1)

iii. Define the stability factor and its dependency on the different parameters. (2 marks, BL: L2, PO: 1)

iv. Derive the relation between the current gain of the CB and CE configurations of BJT. (2 marks, BL: L2, PO: 2)

v. What is the difference between enhancement and depletion type MOSFET. (2 marks, BL: L2, PO: 1)

vi. Find the value of drain current at Q-point if maximum drain current is $2A$, applied $V_{gs} = -4V$ and pinch-off voltage is $-8V$. Validate it by showing the Q-point on the characteristics. (2 marks, BL: L3, PO: 3)

vii. Write the name of parameters of Op-Amp and their ideal and practical values (**five at least**). (2 marks, BL: L2, PO: 1)

viii. What do you mean by the virtual short and virtual ground condition. (2 marks, BL: L2, PO: 2)

ix. Make an electrical circuit for performing the operation of NOT gate and validate the operation (2 marks, BL: L2, PO: 1)

x. Draw a logic circuit for $f(A, B, C) = 1 + \bar{A}B + A\bar{B} + ABC + AB\bar{C}$. (2 marks, BL: L2, PO: 1)

Q2 (a) What are the different types of currents in the semiconductors? Explain and derive the expression for all in a PN junction diode. (2.5 marks, BL: L3, PO: 2)

(b) Determine the currents in each branch in the network shown in **Fig. A**. (2.5 marks, BL: L3, PO: 3)

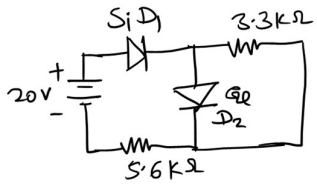


Fig. A [Q2(b)]

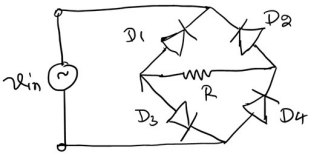


Fig. B [Q2(c)]

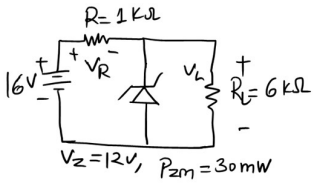


Fig. C [Q2(d)]

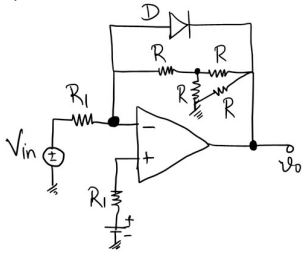


Fig. D [Q5(a)]

PTO

(c) Draw the output waveform of the circuit shown in **Fig. B**, if output voltage is calculated across the resistance R. Also, calculate the related performance parameters, if applicable. (2.5 marks, BL: L3, PO: 3)

(d) For the Zener diode network of **Fig. C**, determine V_L, V_R, I_z, and P_Z. (2.5 marks, BL: L3, PO: 2)

Q3 (a) Determine the Q-point for the potential divider circuit of BJT containing the circuit elements as $R_1 = 39K\Omega, R_2 = 3.9k\Omega, V_{CC} = 22V, R_c = 10k\Omega, R_E = 1.5k\Omega, \beta = 100$ and consider the values of coupling capacitors as $C_i = 10\mu F$, $C_o = 10\mu F$ and $C_E = 50\mu F$. (5 marks, BL: L3, PO: 2)

OR

Explain the Fixed Bias configuration and derive its stability factor. (5 marks, BL: L2, PO: 2)

(b) Explain the working and operation of Darlington pair. What is the need of multistage amplifier? (5 marks, BL: L2, PO: 1)

OR

What is the need of biasing? Explain with the characteristics and operation of BJT. (5 marks, BL: L2, PO: 1)

Q4 (a) Explain the working and operation of n −channel enhancement type of MOSFET. Draw its characteristics. What do you mean by the channel length modulation in MOSFET? (5 marks, BL: L2, PO: 1)

(b) In a self-bias configuration of a JFET, given, $V_{DD} = 20V, R_D = 3.3k\Omega, R_s = 1k\Omega, R_{in} = 1M\Omega, V_p = -6V, I_{DSS} = 8mA$. Determine, $V_{GSQ}, I_{GQ}, V_{DS}, V_S$ and V_G. (5 marks, BL: L3, PO: 2)

OR

How to calculate the Q-point in potential divider configuration of JFET? (5 marks, BL: L3, PO: 2)

Q5 (a) Draw the output waveform for the circuit shown in Fig. D, $R = 2k\Omega, R_1 = 2\Omega, V_{in} = 20V$ and $V_{ref} = 2V$. (5 marks, BL: L3, PO: 2)

(b) Draw the circuit of a differentiator and explain its operation. Apply a signal $x(t) = 2\sin(200\pi t)$ at its input and draw its output. (5 marks, BL: L3, PO: 2)

Solution manual

Q1 attempt all (20 marks)

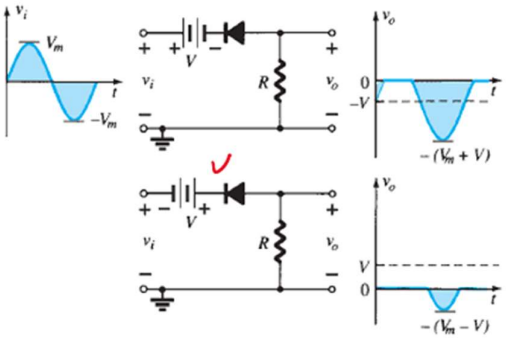
i. The reverse saturation current is of $20\mu A$ in a PN junction diode at room temperature. What will be its values after 20° rise in the temperature? (2 marks, BL: L3, PO: 2)

Solution

Reverse current doubles for every 10° rise in the temperature. So, it is $80\mu A$.

ii Draw the circuit of positive clipper with the offset value of 2V and explain its operation. (2 marks, BL: L2, PO: 1)

Solution



iii. Define the stability factor and its dependency on the different parameters. (2 marks, BL: L2, PO: 1)

Solution

Stability factor defines the stability of collector current in transistor over the variations in the temperature dependent parameters. This can be defined in three ways as follows.

$$S = \frac{dI_c}{dI_{co}}$$

$$S = \frac{dI_c}{d\beta}$$

$$S = \frac{dI_c}{dV_{BE}}$$

iv. Derive the relation between the current gain of the CB and CE configurations of BJT. (2 marks, BL: L2, PO: 2)

Solution

$I_C = \alpha I_E + I_{CBO}$

$I_C = \alpha(I_C + I_B) + I_{CBO}$

$I_C - \alpha I_C = \alpha I_B + I_{CBO}$

$(1-\alpha) I_C = \alpha I_B + I_{CBO}$

$I_C = \left(\frac{\alpha}{(1-\alpha)}\right) I_B + \frac{1}{(1-\alpha)} I_{CBO}$

$I_C = \beta I_B + (1+\beta) I_{CBO}$

Relation between currents in CB & CE Configuration.

CG. in C.B. $\rightarrow \beta = \frac{\alpha}{1-\alpha}$ CG. in C.E.

v. What is the difference between enhancement and depletion type MOSFET. (2 marks, BL: L2, PO: 1)

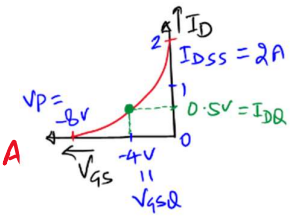
Solution

Channel is already formed in the depletion type of MOSFET. Channel is formed using biasing in the enhancement type of MOSFET.

vi. Find the value of drain current at Q-point if maximum drain current is $2A$, applied $V_{gs} = -4V$ and pinch-off voltage is $-8V$. Validate it by showing the Q-point on the characteristics. (2 marks, BL: L3, PO: 3)

Given $V_{GS} = -4V$ & $V_P = -8V$ & $I_{DSS} = 2A$

from $I_D = I_{DSS}\left(1 - \frac{V_{GS}}{V_P}\right)^2 = 2\left(1 - \frac{4}{8}\right)^2 = 2\left(\frac{1}{4}\right) = 0.5A$



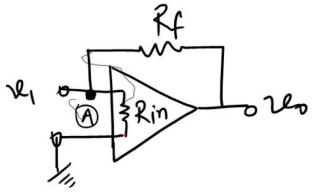
vii. Write the name of parameters of Op-Amp and their ideal and practical values (**five at least**). (2 marks, BL: L2, PO: 1)

Solution

Parameter	Ideal op-Amp.	Practical op-Amp.
① R_i	∞	very high.
② R_o	0	very low
③ Ave	∞	very high
④ CMRR	∞	very high
⑤ SR	∞	very high:
⑥ Input offset	0	very smal

viii. What do you mean by the virtual short and virtual ground condition. (2 marks, BL: L2, PO: 2)
Solution

Virtual short/Virtual Ground



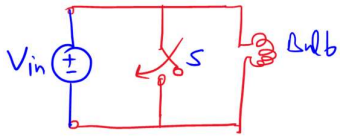
Ideally; $R_{in} = \infty$

So from:- $Ave = \frac{v_o}{v_i - v_o} \Rightarrow Ave \approx \infty$

at node (A) $\rightarrow v_i = 0V$

This is called virtual short/ground Gnd.

ix. Make an electrical circuit for performing the operation of NOT gate and validate the operation (2 marks, BL: L2, PO: 1)



V_{in}	S	Bulb
1	off	ON
1	ON	OFF

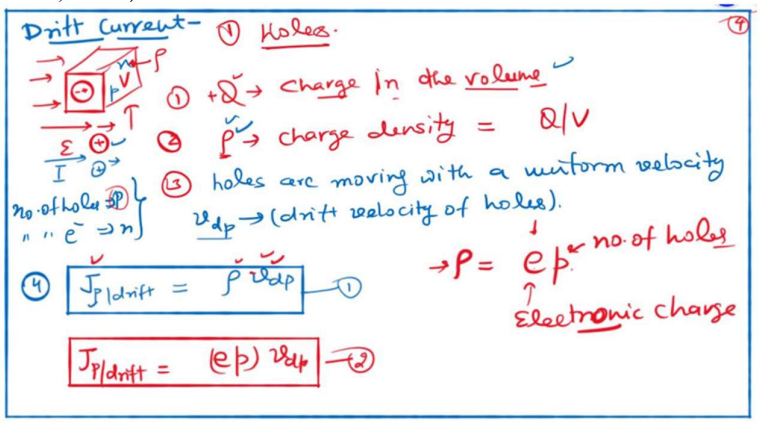
x. Draw a logic circuit for $f(A, B, C) = 1 + \bar{A}B + A\bar{B} + ABC + AB\bar{C}$. (2 marks, BL: L2, PO: 1)

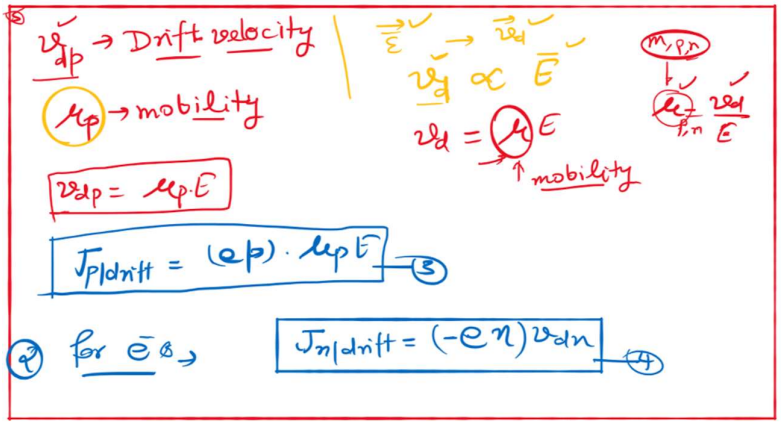
from Entity-

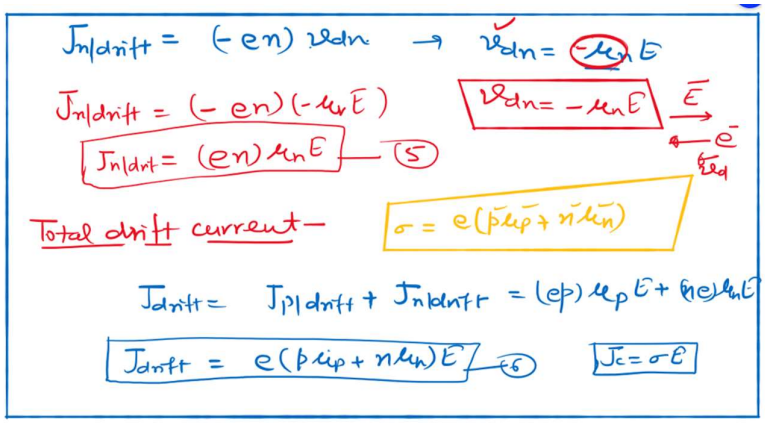
$1 + x = 1$

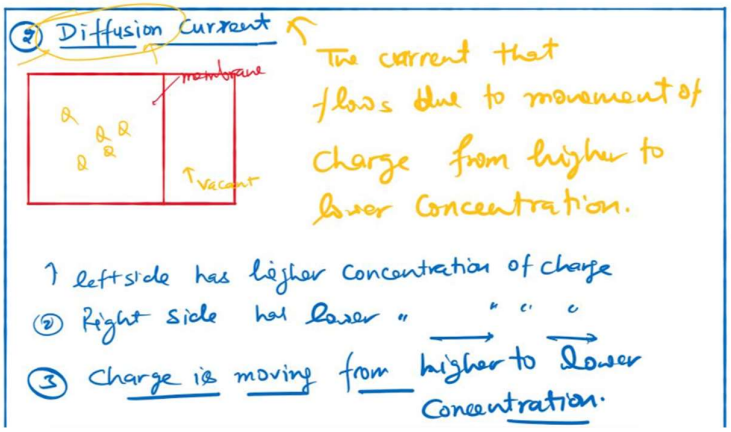
$x = 1$ ——— $F(A,B,C)$

Q2 (a) What are the different types of currents in the semiconductors? Explain and derive the expression for all in a PN junction diode. (2.5=1+1.5 marks, BL: L3, PO: 2)





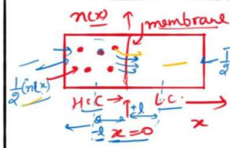




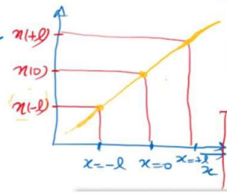
③ Diffusion Current-

① There is flow of charge carriers from higher to lower concentration side.

② The motion of charge particles generates a current which is called "Diffusion current".

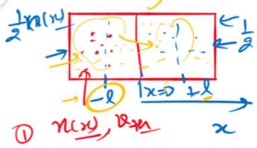


① $n(x)$, v_{th}



② net flow of charge f_n

$$f_n = \frac{1}{2} n(-l) v_{th} - \frac{1}{2} n(+l) v_{th} \quad \text{①}$$



① $n(x)$, v_{th}

→ ① membrane is not broken

② membrane is broken.

↳ (i) flow of charge from H.C. to L.C.

(ii) After some time charge will come under steady state or (uniformly distrib.)

net flow of charge

$$f_n = \frac{1}{2} n(-l) v_{th} - \frac{1}{2} n(l) v_{th} \quad \text{①}$$

$$f_n = \frac{1}{2} [n(-l) - n(l)] v_{th} \quad \text{②}$$

using one dimensional Taylor's series expansion.

$$n(l) = n(0) + l\frac{dn}{dx} + \frac{l^2}{2}\frac{d^2n}{dx^2} + \cdots$$

$$n(-l) = n(0) - l\frac{dn}{dx} + \frac{l^2}{2}\frac{d^2n}{dx^2} + \cdots$$

Ignore the higher order terms-

$$f_n = \frac{1}{2} v_{th} \left[\left\{ n(0) - l\frac{dn}{dx} \right\} - \left\{ n(0) + l\frac{dn}{dx} \right\} \right]$$

$$f_n = \frac{1}{2} v_{th} \left[-2l\frac{dn}{dx} \right] = -l v_{th} \frac{dn}{dx}$$

$$f_n = -l v_{th} \frac{dn}{dx} \quad \text{③}$$

① For e⁻s-

$$f_n = -l v_{th} \frac{dn}{dx} \quad \text{③}$$

D_n → diffusion coefficient

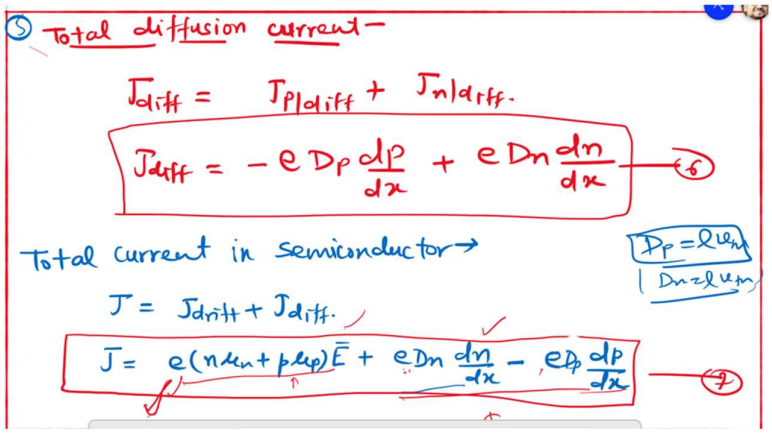
n → no. of e⁻s

$$J_{n|diff} = e D_n \frac{dn}{dx} \quad \text{④}$$

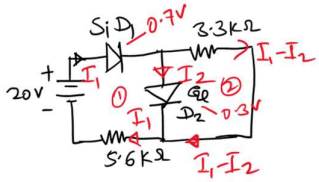
② For holes- $f_n = -l v_{th} \frac{dp}{dx}$ ⇒ p ⇒ no. of holes.

D_p → Diffusion coeff.

$$J_{p|diff} = -e D_p \frac{dp}{dx} \quad \text{⑤}$$



(b) Determine the currents in each branch in the network shown in figure 1. (2.5 marks, BL: L3, PO: 3)



Applying KVL in loop ①

$-20 + 0.7 + 0.3 + 5.6\times10^3 I_1 = 0$

$\Rightarrow I_1 = \frac{19}{5.6}\,mA = 3.39\,mA$

In loop ②

$I_1 - I_2 = \frac{0.3}{3.3\times10^3}$

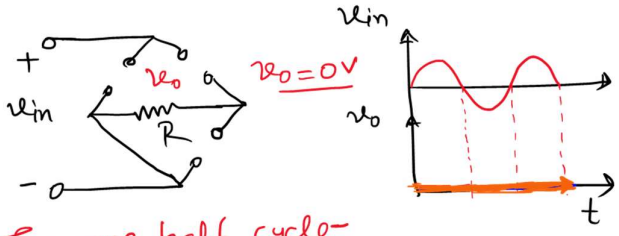
$I_1 - I_2 = 90.90\,\mu A$

and $I_1 - I_2 = 90.9\,\mu A \Rightarrow I_2 = (3.39 - 0.0909)\,mA = 3.2971\,mA$

(c) Draw the output waveform of the circuit shown in **Fig. B**, if output voltage is calculated across the resistance R. Also, calculate the related performance parameters, if applicable. (2.5 marks, BL: L3, PO: 3)

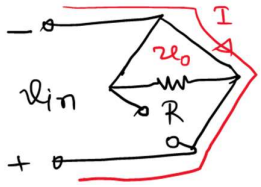
For +ve half cycle–

D_1, D_2 & D_4 are open ckted.



For –ve half cycle–

D_1, D_2 & D_4 are shortckted.

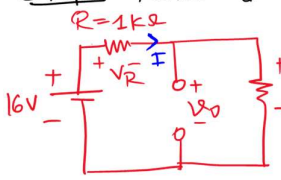


There is no current in R due to S.C.

hence $v_o = 0V$

(d) For the Zener diode network of **Fig. C**, determine V_L, V_R, I_Z, and P_Z. (2.5 marks, BL: L3, PO: 2)

Step1:- Remove zener diode and calculate the open ckt voltage.



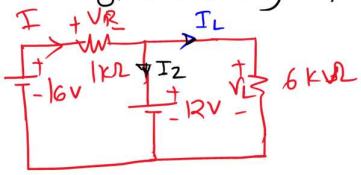
$-16 + I\times10^3 + 6\times10^3 I = 0$

$\Rightarrow I = \frac{16}{7} = 2.28\ mA$

$\Rightarrow V_L = I \times R_L = 13.71V$

So, $\Rightarrow V_Z = 12V < V_L$

Step2:- Since $V_L > V_Z$, hence zener diode must be replaced by the battery of value V_Z.



hence $V_L = 12V$

$\Rightarrow -16 + I\times10^3 + 12 = 0$

$I = \frac{4}{10^3} = 4mA$

$\Rightarrow I_L = \frac{12}{6K} = 2mA$

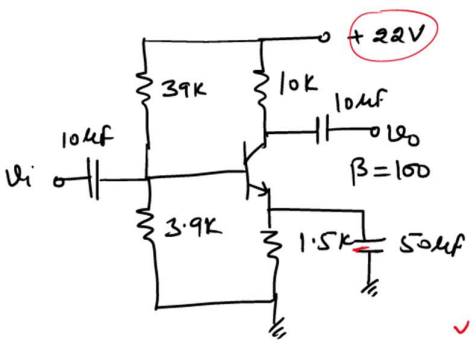
$\Rightarrow I_2 = I - I_L = 4 - 2 = 2mA$

$\Rightarrow V_R = 4V$

$P_Z = V_Z I_Z$

$P_Z = 24\ mW$

Q3 (a) Determine the Q-point for the potential divider circuit of BJT containing the circuit elements as $R_1 = 39K\Omega, R_2 = 3.9k\Omega, V_{CC} = 22V, R_c = 10k\Omega, R_E = 1.5k\Omega, \beta = 100$ and consider the values of coupling capacitors as $C_i = 10\mu F$, $C_o = 10\mu F$ and $C_E = 50\mu F$. (5 marks, BL: L3, PO: 2)



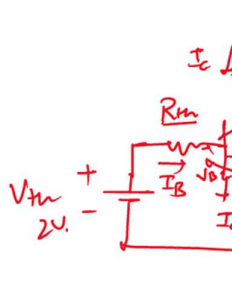
Solution →

For DC analysis, remove all capacitances.

$X_C \propto \frac{1}{\omega C} \approx \infty$

$R_{th} = \frac{39\times3.9}{39+3.9}\ k\Omega$

$V_{th} = \frac{V_{cc}R_2}{R_1+R_2} = \frac{22\times3.9}{39+3.9}\ V$



$R_{th} = 3.55\ K$

$V_{th} = 2V$

$I_E = I_B + I_C$

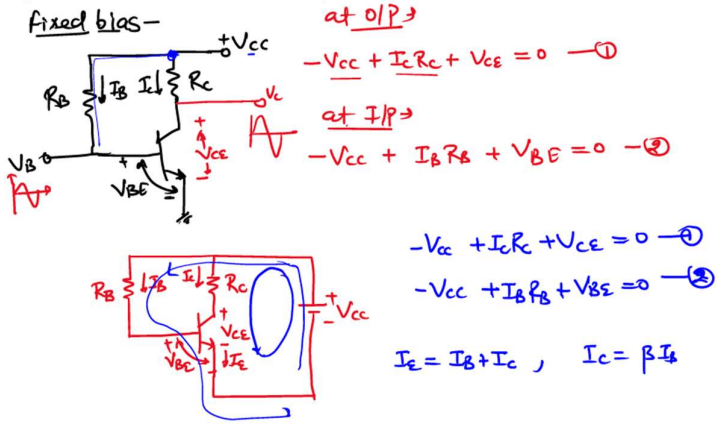
$-22 + I_C\times10\times10^3 + V_{CE} + I_E\times1.5\times10^3 = 0$ ... (1)

$-2 + I_B\times3.55\times10^3 + V_{BE} + I_E\times1.5\times10^3 = 0$ ... (2)

$I_C = \beta I_B + I_{CEO}$

OR

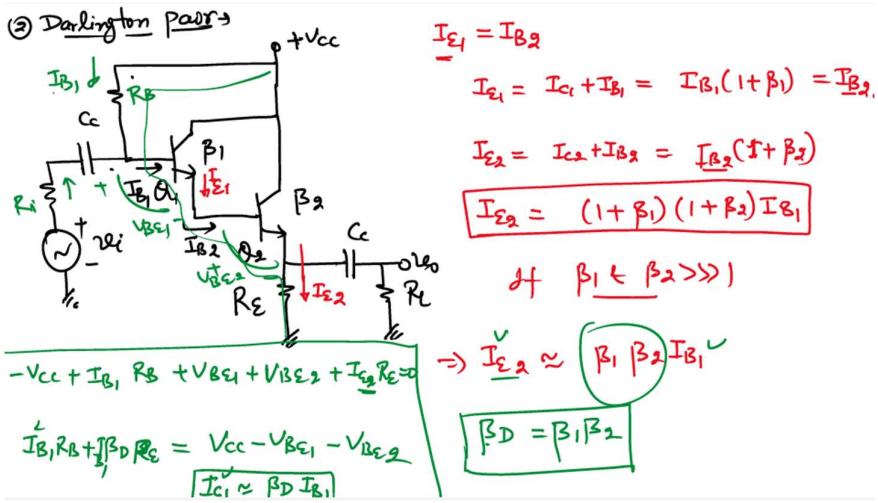
Explain the Fixed Bias configuration and derive its stability factor. (5 marks, BL: L2, PO: 2)



The stability factor can be calculated using the following formulation

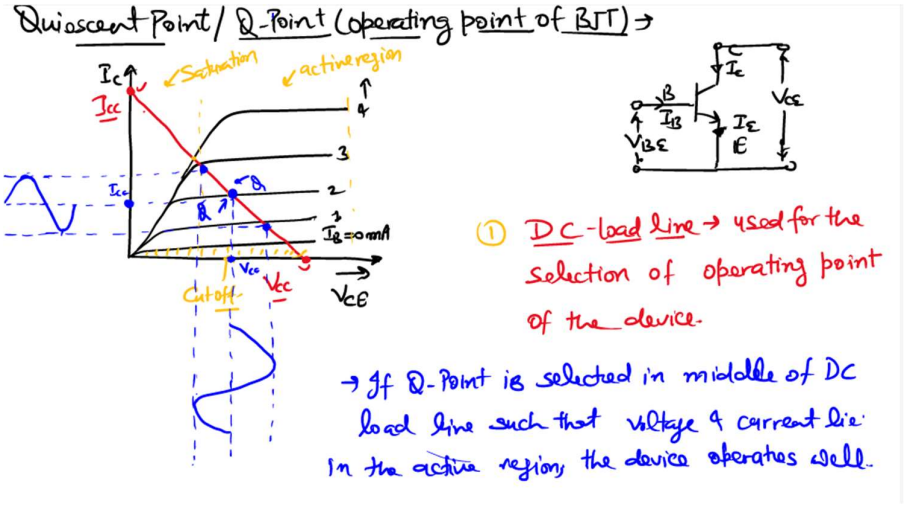
$$S = \frac{(1+\beta)}{\left(1-\beta\frac{\partial I_B}{\partial I_C}\right)}$$

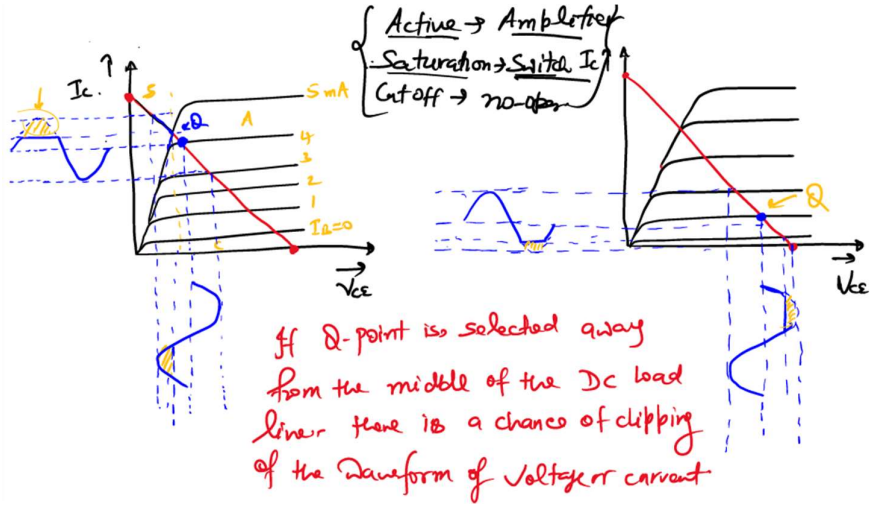
(b) Explain the working and operation of Darlington pair. What is the need of multistage amplifier? (5 marks, BL: L2, PO: 1)



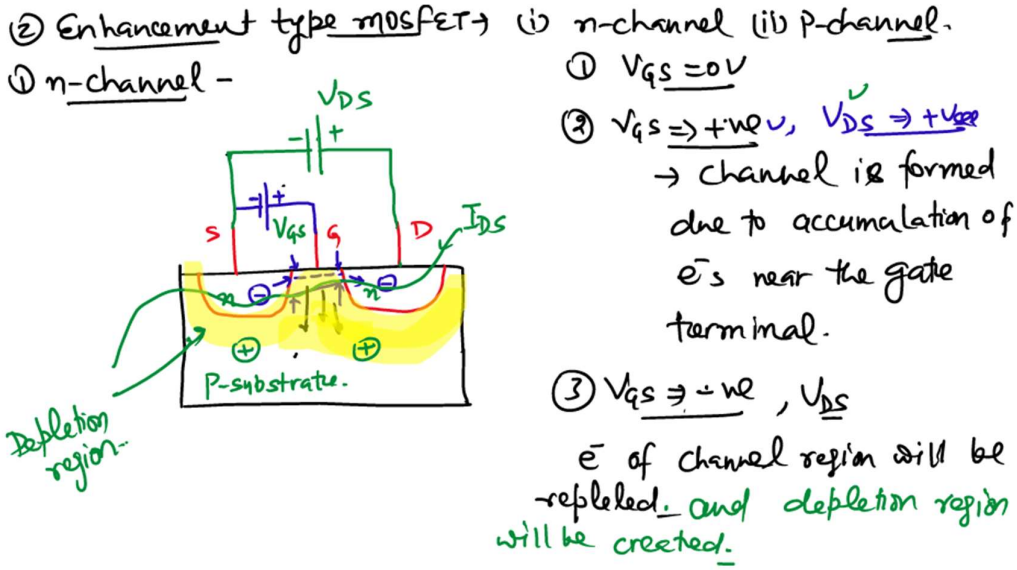
OR

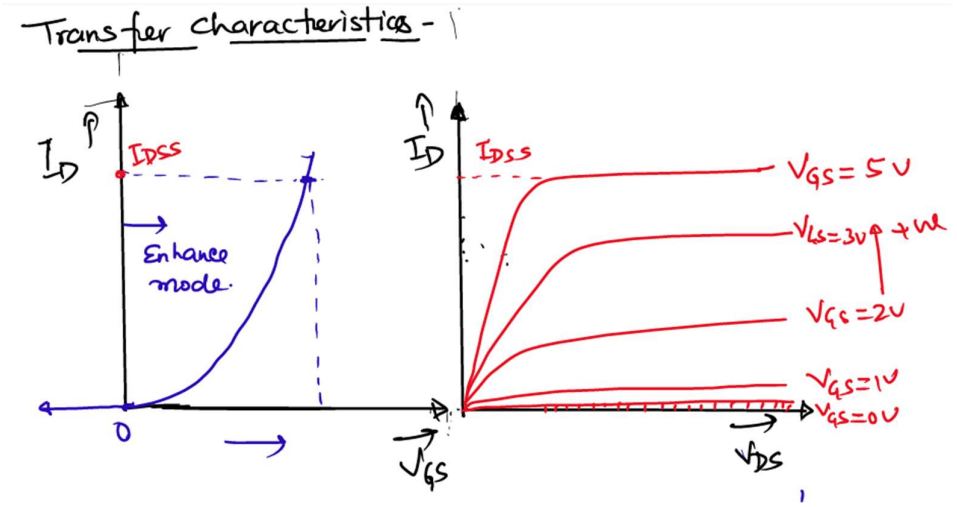
What is the need of biasing? Explain with the characteristics and operation of BJT. (5 marks, BL: L2, PO: 1)





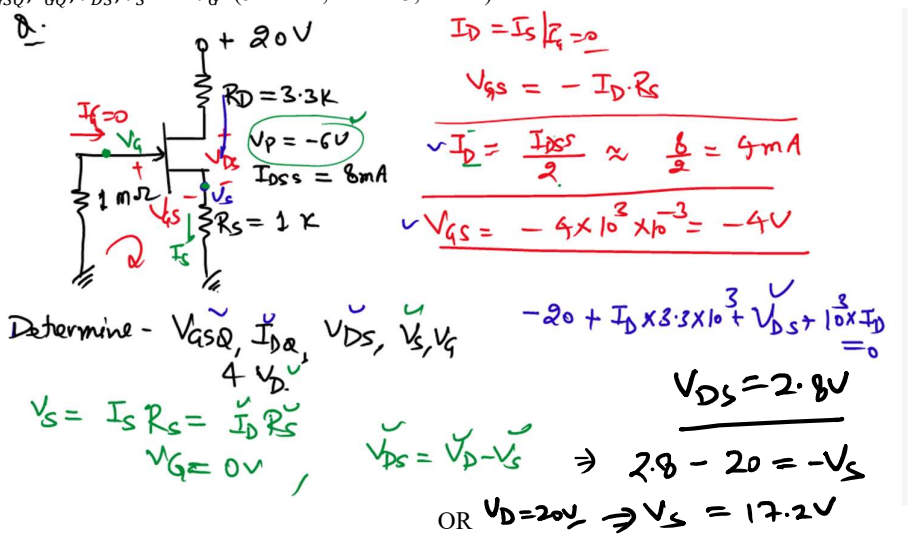
Q4 (a) Explain the working and operation of n −channel enhancement type of MOSFET. Draw its characteristics. What do you mean by the channel length modulation in MOSFET? (5=2+2+1 marks, BL: L2, PO: 1)



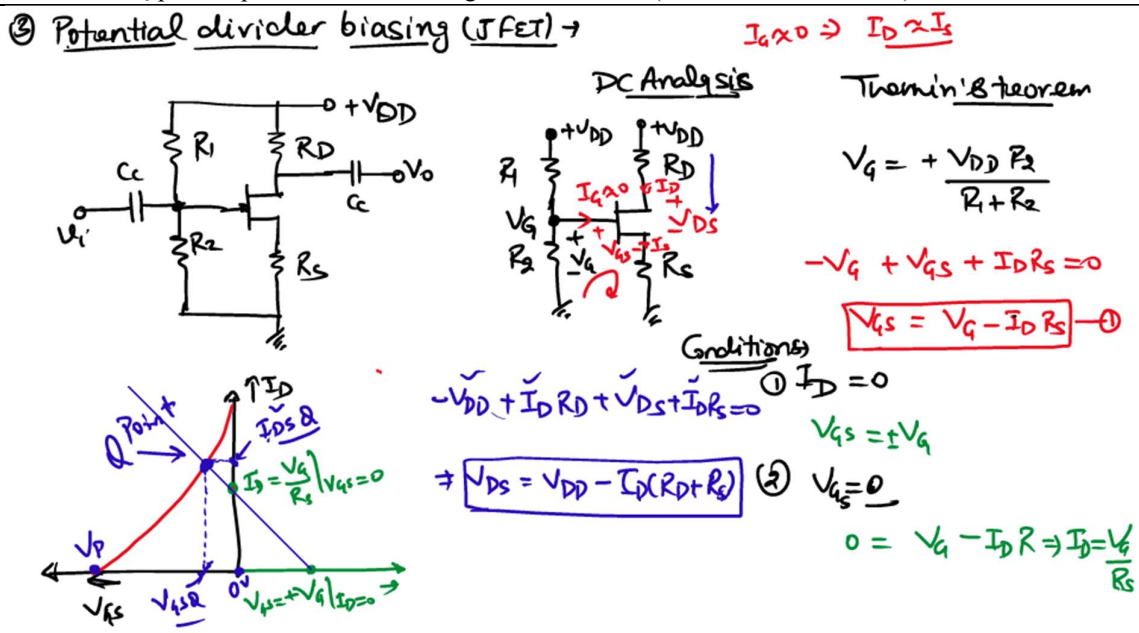


Variation in the length of the channel by applying the voltage on Gate terminal is called as channel length modulation.

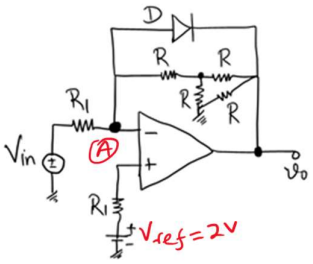
(b) In a self-bias configuration of a JFET, given, $V_{DD} = 20V, R_D = 3.3k\Omega, R_s = 1k\Omega, R_{in} = 1M\Omega, V_p = -6V, I_{DSS} = 8mA$. Determine, $V_{GSQ}, I_{GQ}, V_{DS}, V_S$ and V_G. (5 marks, BL: L3, PO: 2)



How to calculate the Q-point in potential divider configuration of JFET? (5 marks, BL: L3, PO: 2)



Q5 (a) Draw the output waveform for the circuit shown in Fig. D, $R = 2k\Omega, R_1 = 2\Omega, V_{in} = 20V$ and $V_{ref} = 2V$. (5 marks, BL: L3, PO: 2)

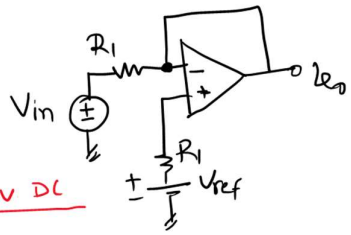


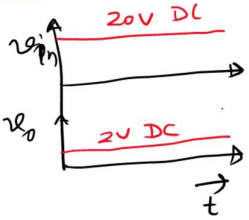
at node (A) →

$V_A = 2V$

→ Diode 'D' is forward biased and provides a short ckted path to resistive network. This makes ckt as shown in Fig. (A).

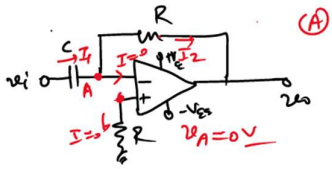
Thus $v_o = V_{ref} = 2V$





(b) Draw the circuit of a differentiator and explain its operation. Apply a signal $x(t) = 2\sin(200\pi t)$ at its input and draw its output. (5=3+2 marks, BL: L3, PO: 2)

Differentiator – (capacitor at down position)



(A) → $I_1 = I_2 \Rightarrow C\dfrac{d(v_i - 0)}{dt} = \dfrac{0 - v_o}{R}$

$\Rightarrow \boxed{v_o = -RC\dfrac{dv_i}{dt}}$

Q. $v_i = \sin t$, calculate v_o for a differentiator ckt.

$\boxed{v_o = -RC\cos t}$

Q $v_i = u(t) - u(t-1) \rightarrow v_o = ?$

for inverting type of differentiator –

$v_o = -RC\dfrac{dv_o}{dt}$ ⇒ suppose $RC = 1$

$v_o = -2\cos(200\pi t) \times 200\pi = -400\pi\cos(200\pi t)$